전북대학교 반도체 특성화대학 사업단 반도체 콜로퀴엄

NAND Flash Memory
Basic principle, History, and Prospect

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Sung-Il Chang, Ph. D.
CTO, Simulation Solver, Inc.

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- NAND Flash Memory
  - Architecture
  - Basic operation & Reliability
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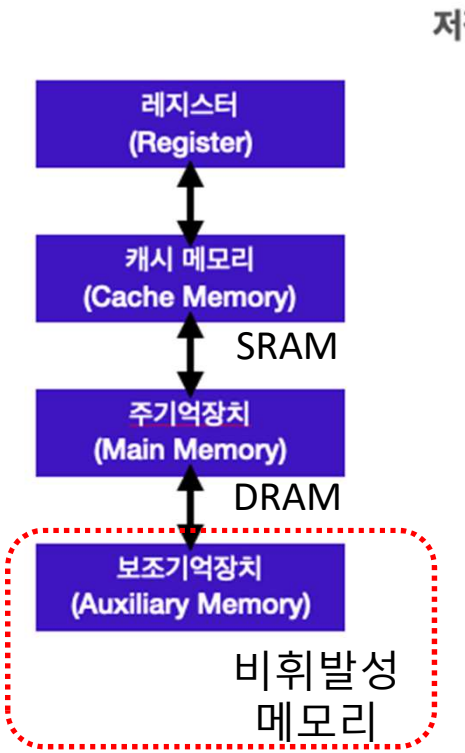
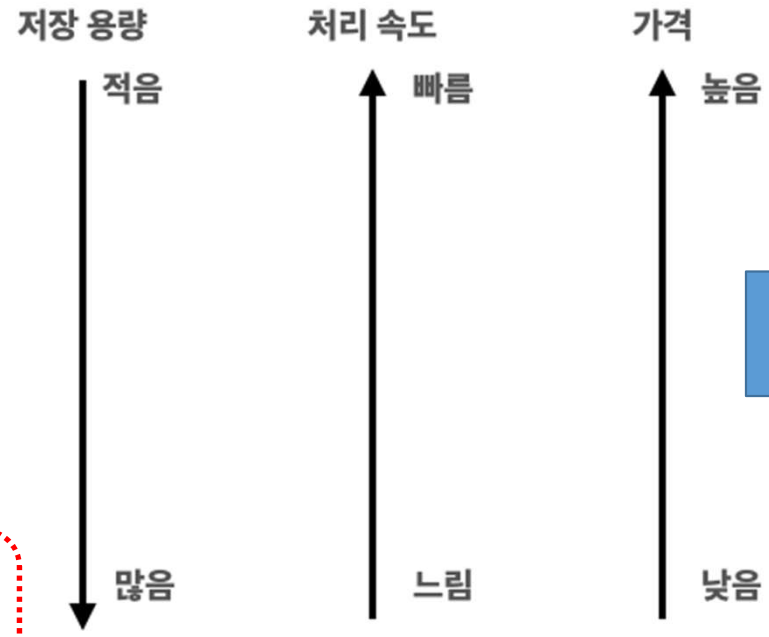
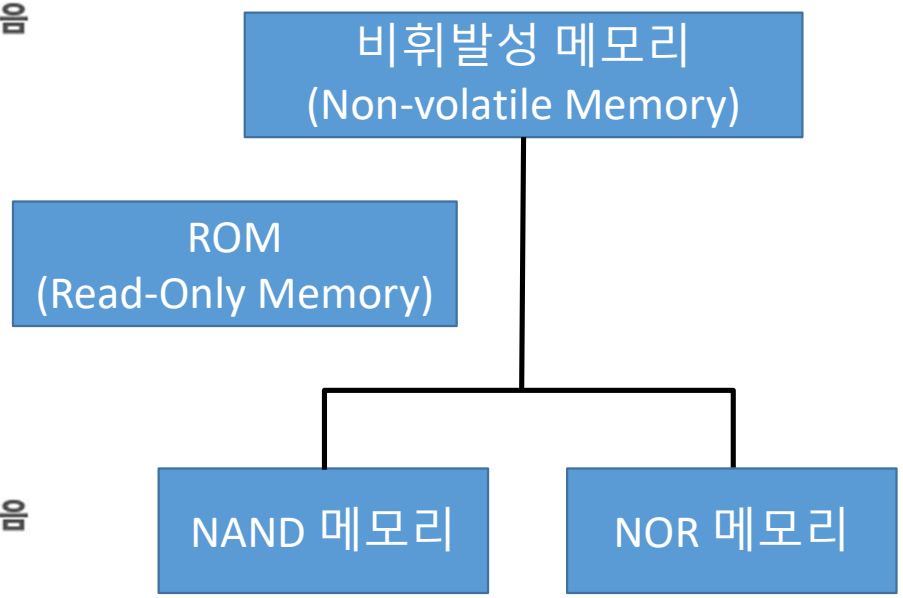
  - Future Prospect

Introduction – Category of Memory Devices

- NAND Flash Memory는 비휘발성, 저가/고집적 보조기억장치용 메모리





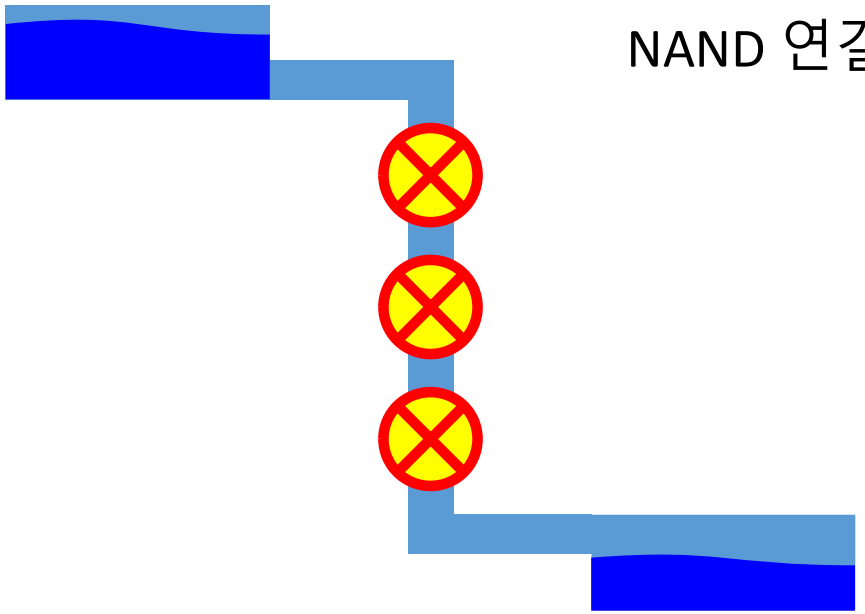


Introduction – NAND vs. NOR

- NAND는 메모리 소자들의 직렬 연결, NOR는 메모리 소자들의 병렬 연결

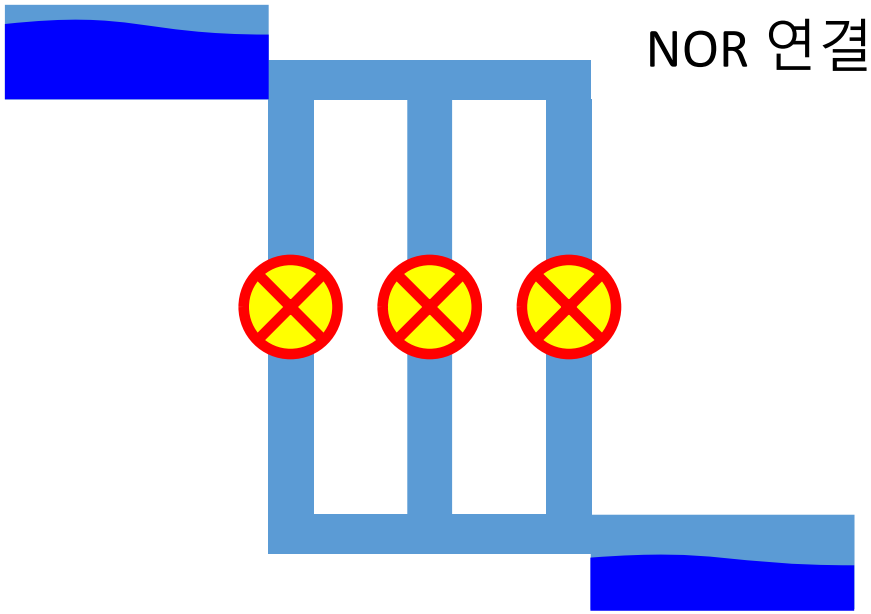
모든 소자가 켜져야 전류가 흐름

NAND 연결



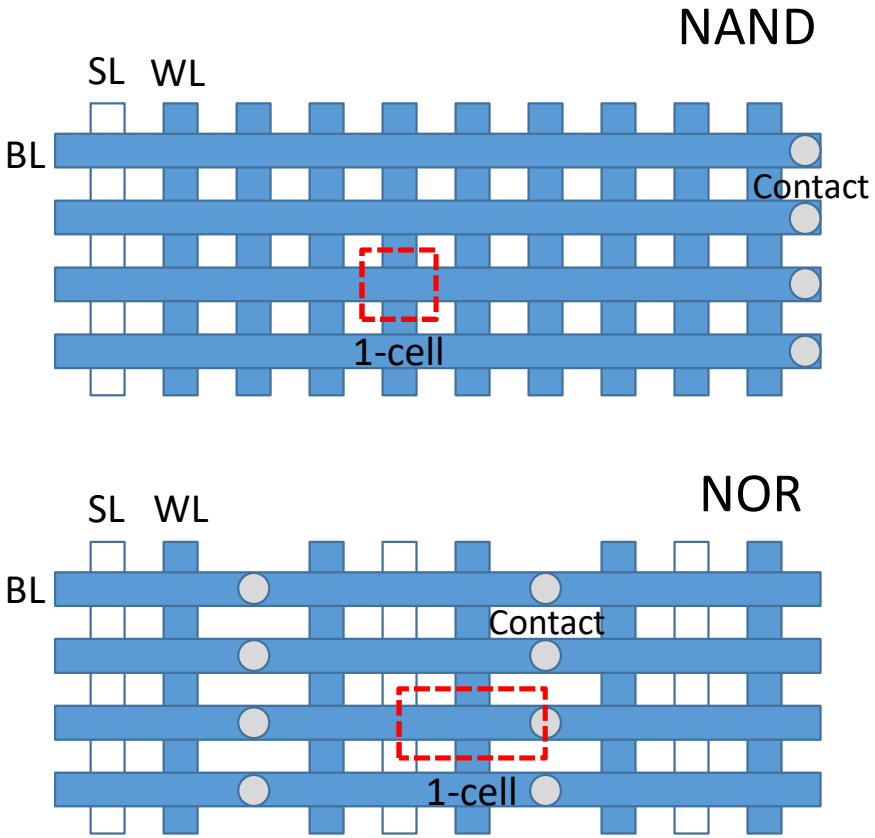
한 소자만 켜져도 전류가 흐름

NOR 연결



Introduction – NAND vs. NOR

항목	NAND	NOR
Cost	낮음	높음
용도	Data 저장	코드 실행
용량	높음	낮음
쓰기 속도	빠름	낮음
읽기 속도	보통	빠름
스탠바이 파워	보통	낮음



Introduction – History of NAND Flash Memory

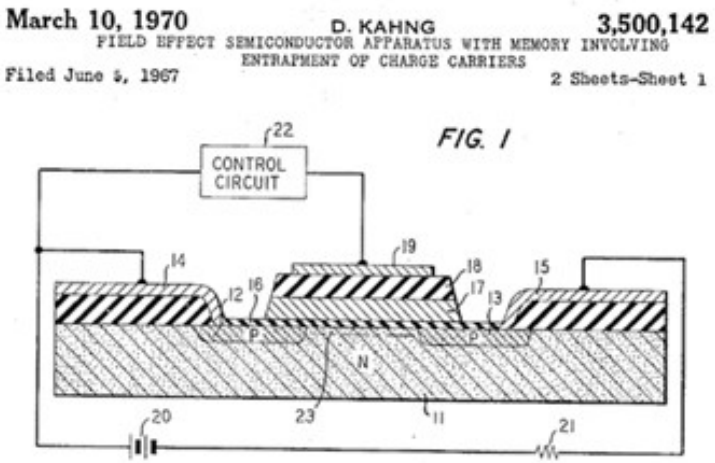
1967 — 강대원/Sze 박사, Bell Lab.
전하 저장을 위한 Floating gate
터널링을 이용한 Write/Erase

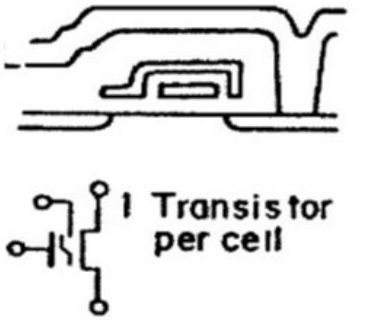
1981 — Masuoka, Toshiba
Flash erasing

1984 — Masuoka, Toshiba
Flash memory 명명

1987 — Masuoka, Toshiba
NAND

1991 — Toshiba
NAND Flash 메모리 상용화


March 10, 1970 D. KAHNG 3,500,142
FIELD EFFECT SEMICONDUCTOR APPARATUS WITH MEMORY INVOLVING ENTRAPMENT OF CHARGE CARRIERS
Filed June 5, 1967 2 Sheets-Sheet 1
FIG. 1
CONTROL CIRCUIT



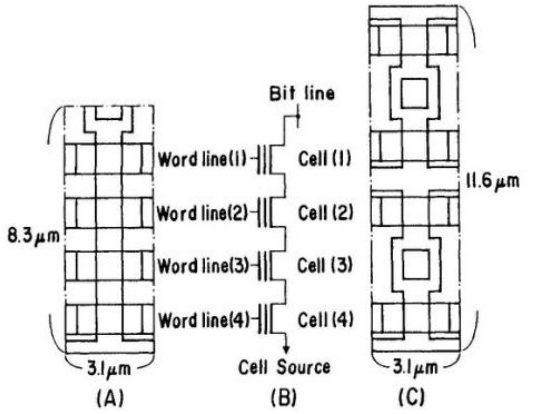
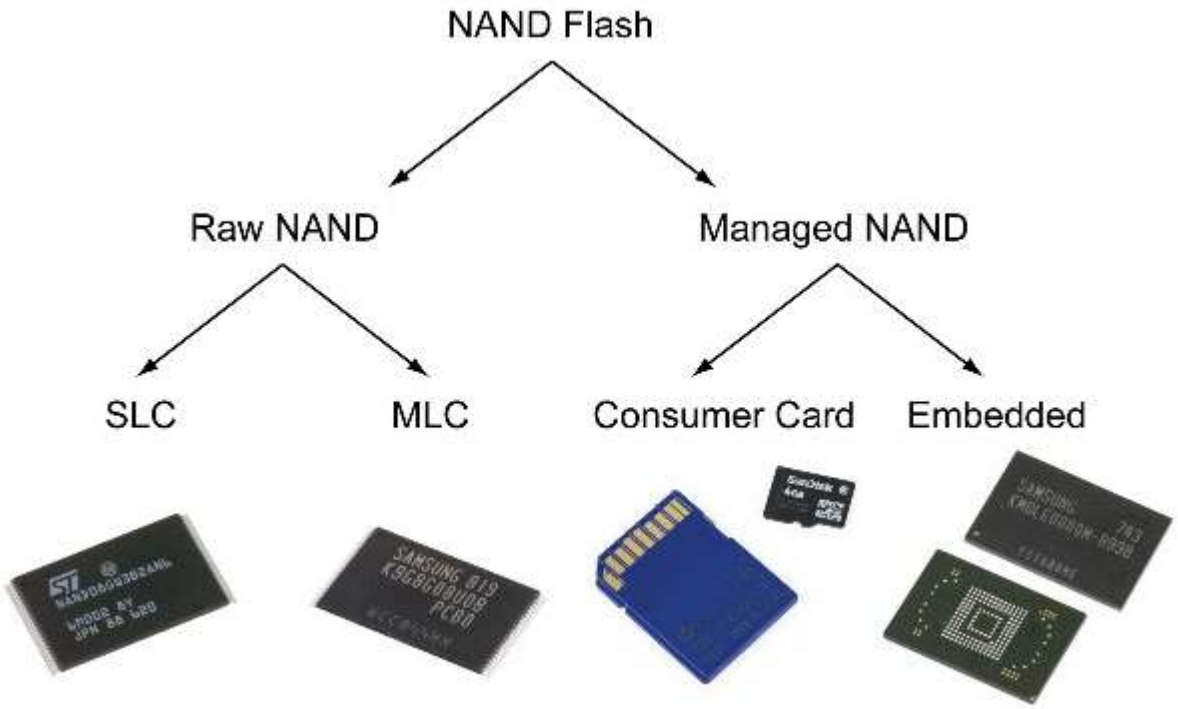
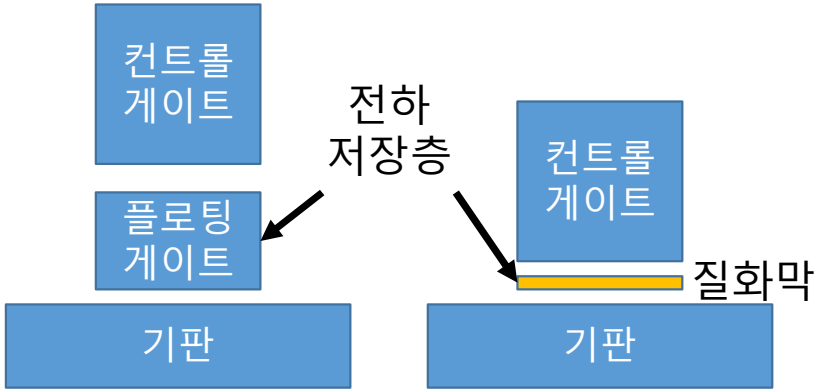


Fig.1. Comparison between a new NAND structure cell (A) and conventional cell (C). Figure (B) shows equivalent circuit of the NAND structure cell having 4 bits.

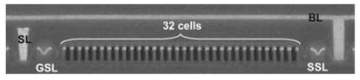
NAND Flash Memory – Category





[플로팅게이트]
(Floating Gate)

[차지트랩플래시]
(Charge Trap Flash)

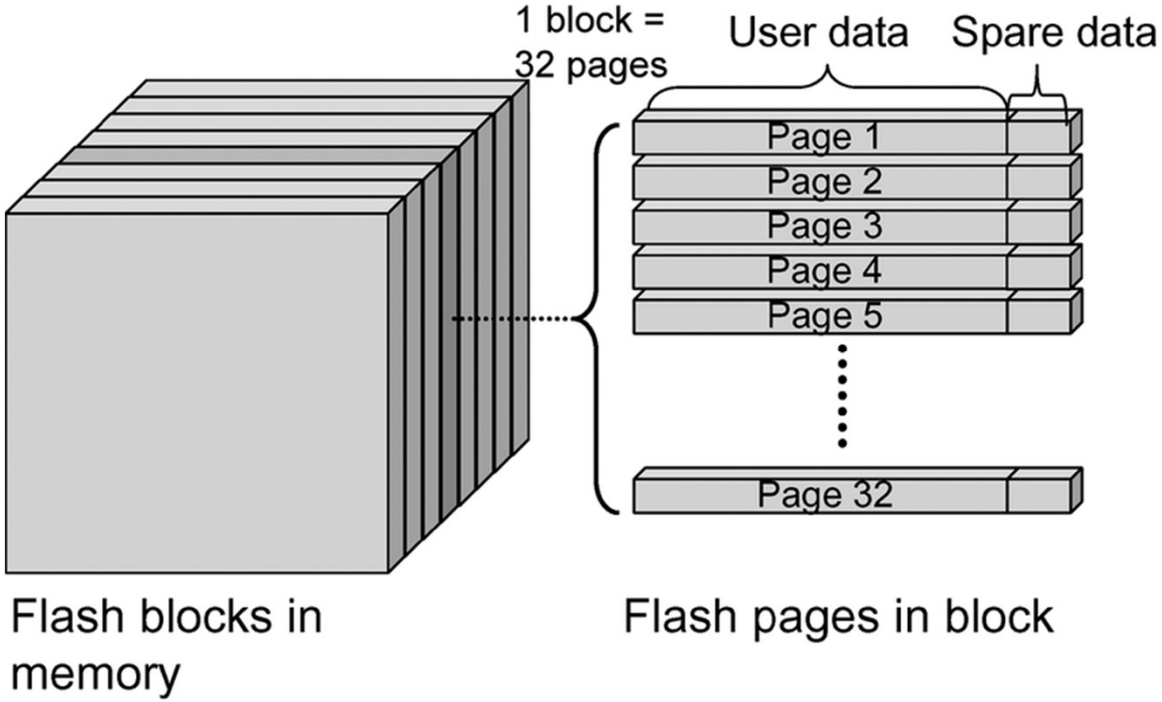


[2D NAND]

[3D NAND]

NAND Flash Memory – Architecture (Block&Page)

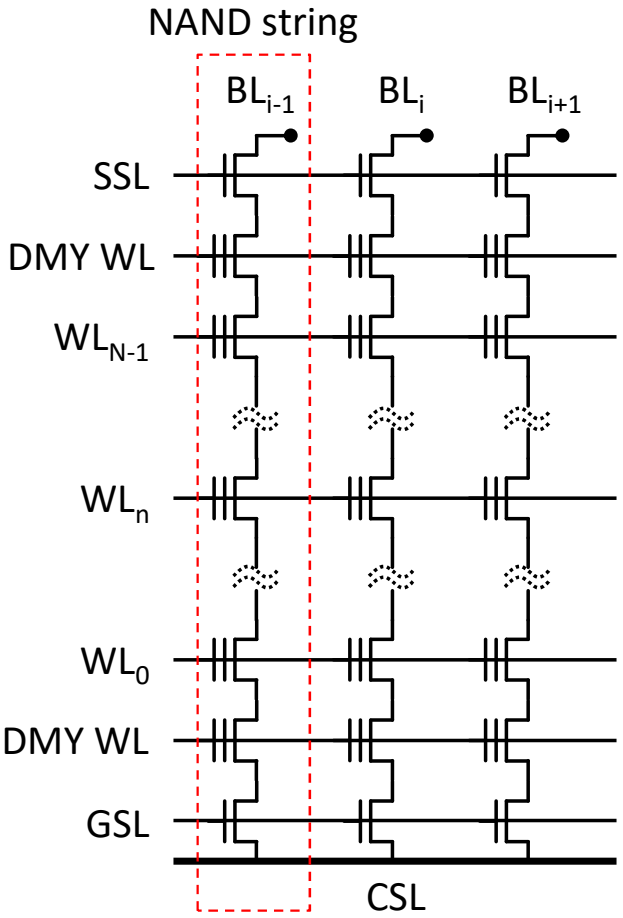
- "터널링"이라는 느린 동작 방식을 극복하고 빠른 동작을 구현하기 위해 page 단위의 읽기/쓰기, block 단위의 지우기



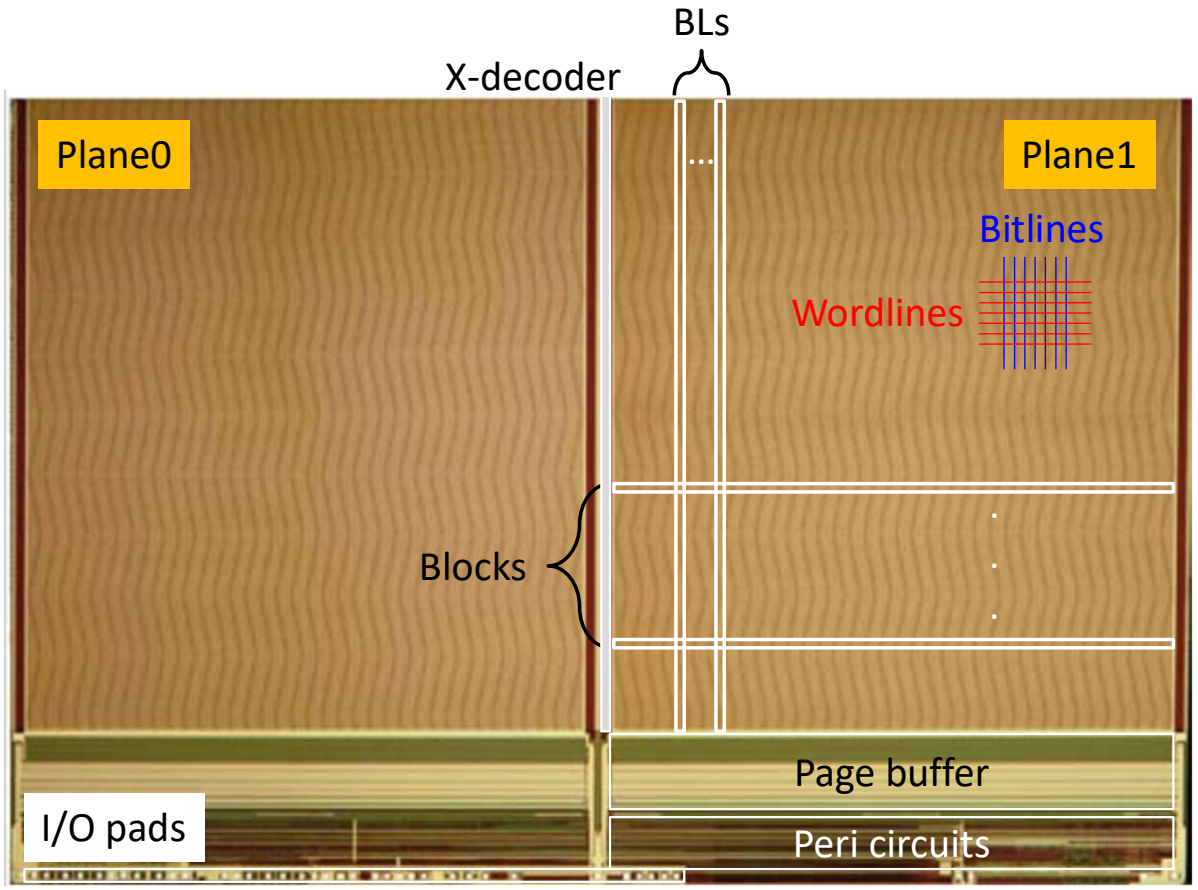
Devices	Samsung 3D V1	Samsung 3D V2
Page Size	8 KB	16 KB
Block Size	384 pages	384 pages
Random Read Time (tR)	49 μs	35 μs
Page Program Time (tPROG)	0.6 ms	0.39 ms
Block Erase Time (tBERS)	4 ms	4 ms

NAND Flash Memory – Structure

구성요소	줄임말	설명
Wordline	WL	메모리 트랜지스터를 켜고 끄는 역할
Bitline	BL	읽기/쓰기할때 data가 들어가고 나가는 역할
String Select Line	SSL	특정 NAND 스트링을 선택할 수 있도록 해 주는 트랜지스터
Ground Select Line	GSL	
Common Source Line	CSL	접지 등의 역할
Dummy WL	DMY WL	선택/메모리 트랜지스터를 보호하기 위한 완충용 트랜지스터
NAND string		CSL부터 BL까지 이르는 cell 및 select 트랜지스터들의 직렬 연결 묶음



NAND Flash Memory – Chip architecture



[Toshiba's 128Gb planar TLC NAND Flash in 2012]

1page: WL 하나에 물려있는 bitline의 개수
1page=16kB=16x1024x8bits
=131,072bits=131,072bitlines

BL의 pitch가 40nm 정도 된다면
Plane 하나의 x축 길이~131,072x40nm
~5.2mm

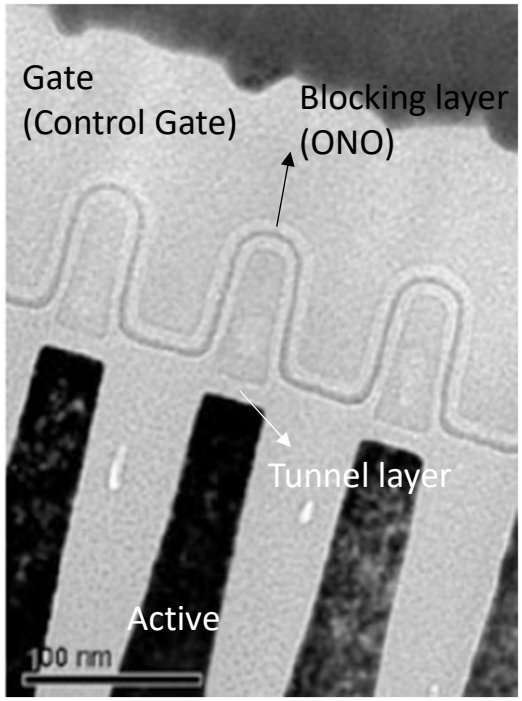
1Block: NAND string 하나에 있는 WL의 개수
만약 string 하나에 64개의 WL이 있고,
2k개의 Block이 있으며,
WL의 pitch가 40nm 정도 된다면
Plane 하나의 y축 길이~64x2048x40nm
~5.2mm

NAND Flash Memory – Structure (Cell transistor)

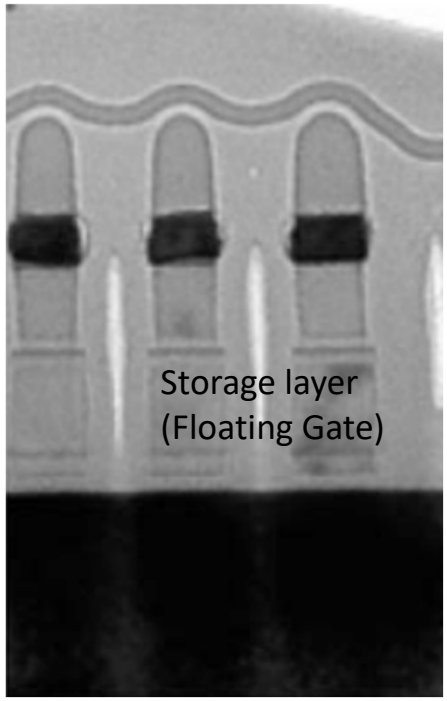
구성요소	설명	2D FG	2D CTF	3D CTF
Active	BL에서 CSL로 전류가 흐르는 길	Single crystal silicon		Poly-Si
Gate	Transistor를 켜고 끄는 역할	Poly-Si	Metal gate or Poly-Si	
Tunnel layer	전하 저장층에 있는 전하가 active로 빠져나가는 것을 막아주는 layer Program/Erase시 전하가 이동하는 통로	SiO_2	SiO_2/SiON 복합막	
Storage layer	전하를 저장하는 layer	Poly-Si	SiN	
Blocking layer	전하 저장층에 있는 전하가 gate로 빠져나가는 것을 막아주는 layer	ONO	SiO_2/High-k 복합막	

NAND Flash Memory – Structure (Cell transistor)

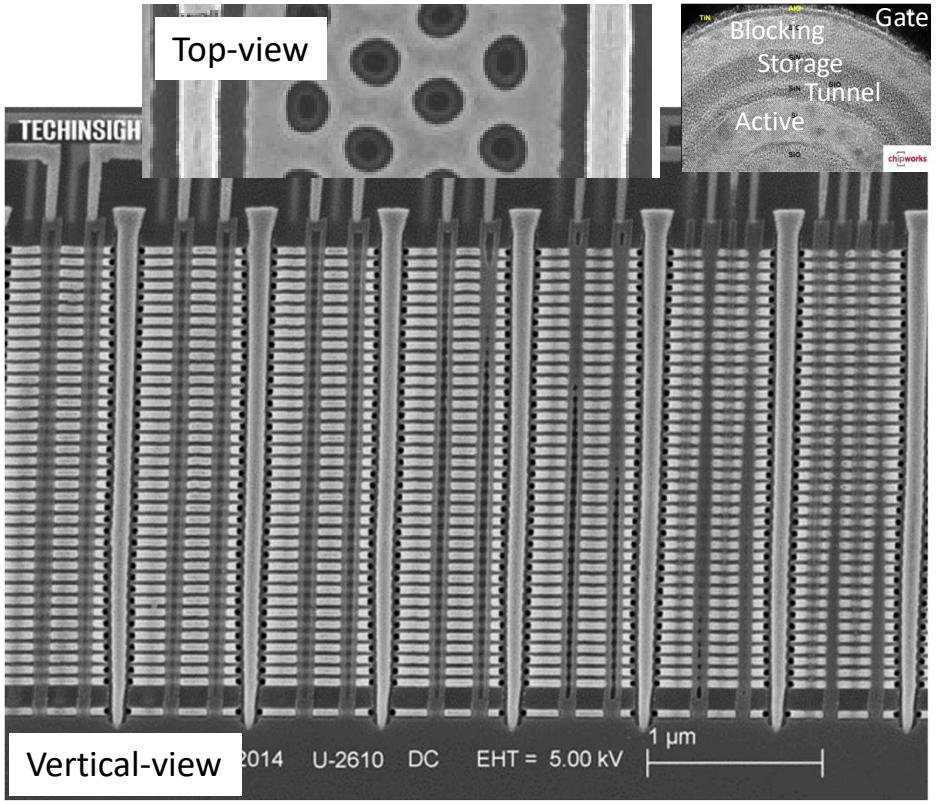
[Active 단면]



[Gate 단면]



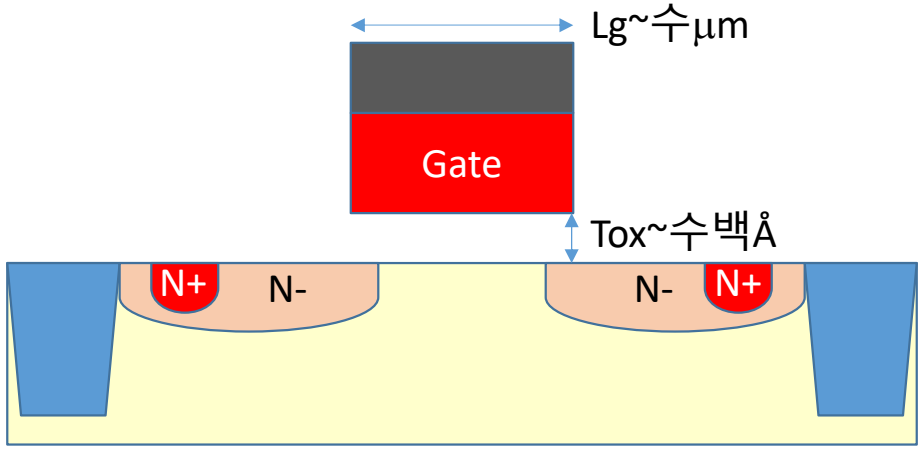
[2D FG Cell]



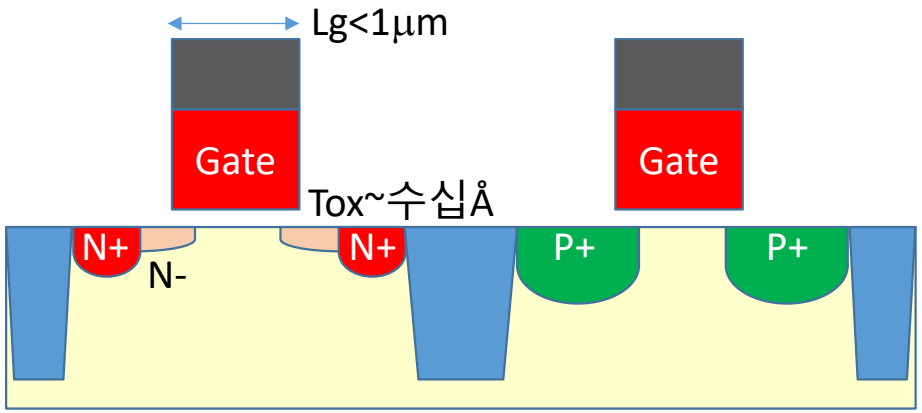
[3D CTF Cell]

NAND Flash Memory – Structure (Core/Peri transistor)

- BL과 연결되는 page buffer, WL과 연결되는 X-decoder 등의 core circuit
- Data I/O를 포함한 다양한 CMOS 회로가 포함된 peri circuit
- Program/erase/read등의 높은 전압을 다루는 high voltage (HV) transistor
- VCC/GND로 동작하는 일반적인 low voltage (LV) transistor

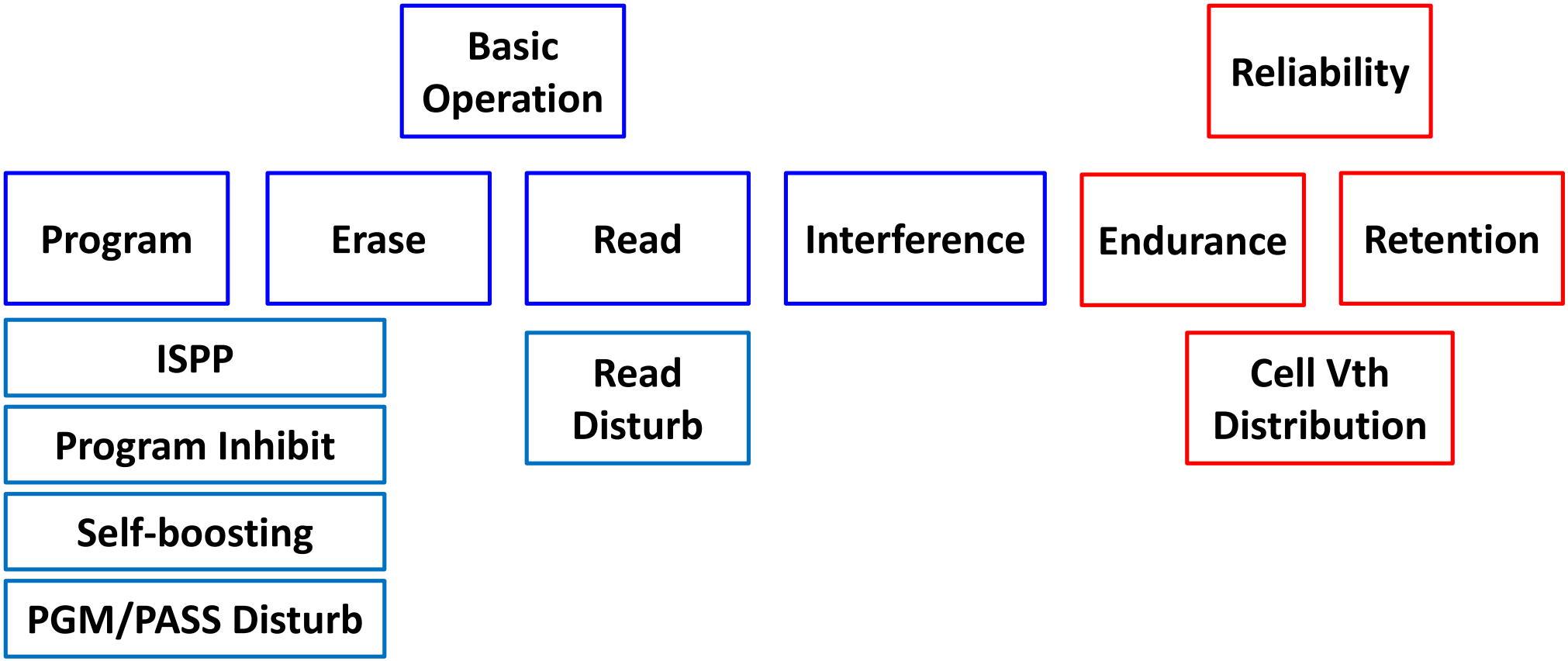


[HV transistor 예시]



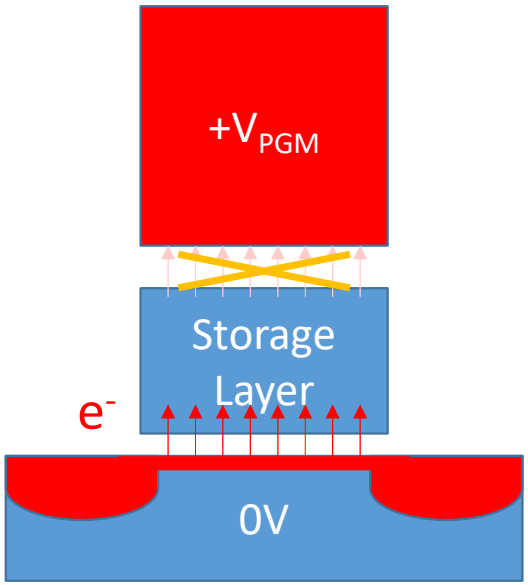
[LV transistor 예시]

NAND Flash Memory – Operation

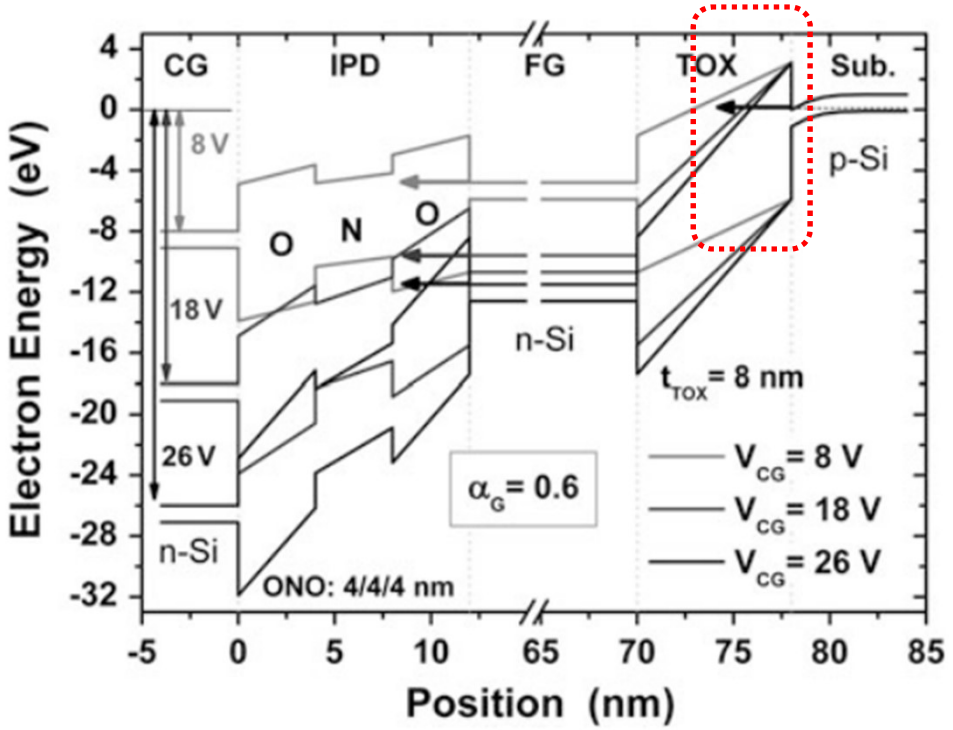


NAND Flash Memory – Basic Operation (Program)

- 프로그램의 주요 원리는 Fowler-Nordheim tunneling



FN tunneling



NAND Flash Memory – Basic Operation (Program)

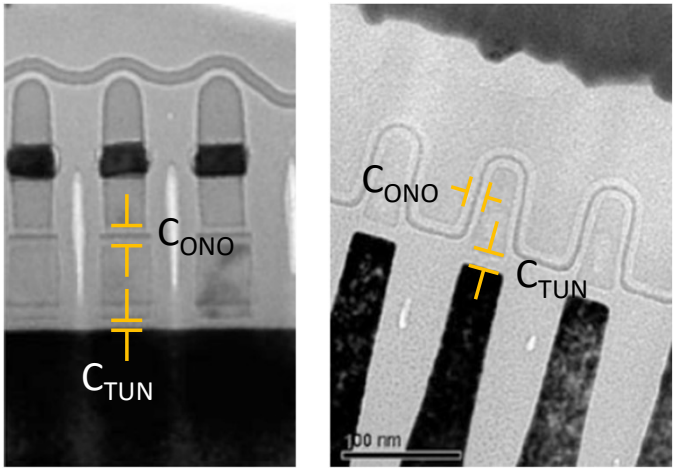
- Tunnel layer에 blocking layer보다 높은 E-field가 걸리도록 소자를 설계
  - Storage layer에 들어간 전하가 Gate로 빠져나가지 않음

$V_{FG}=\alpha V_{CG}$

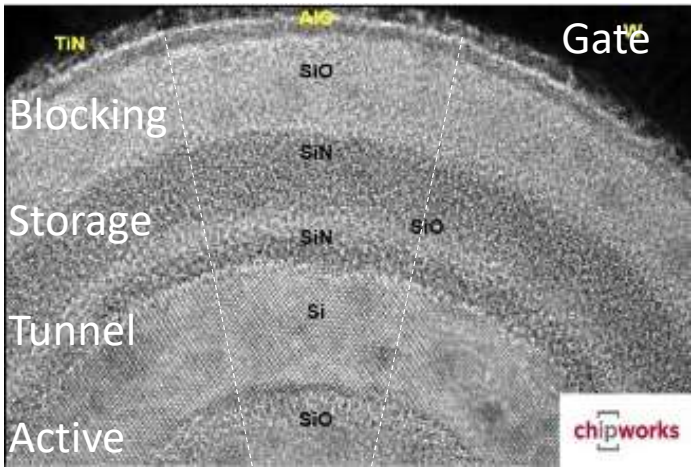
Coupling Ratio (CR)

$$\alpha = \frac{C_{ONO}}{C_{TUN} + C_{ONO}}$$

ONO 면적을 높여서 CR를 증가시킴

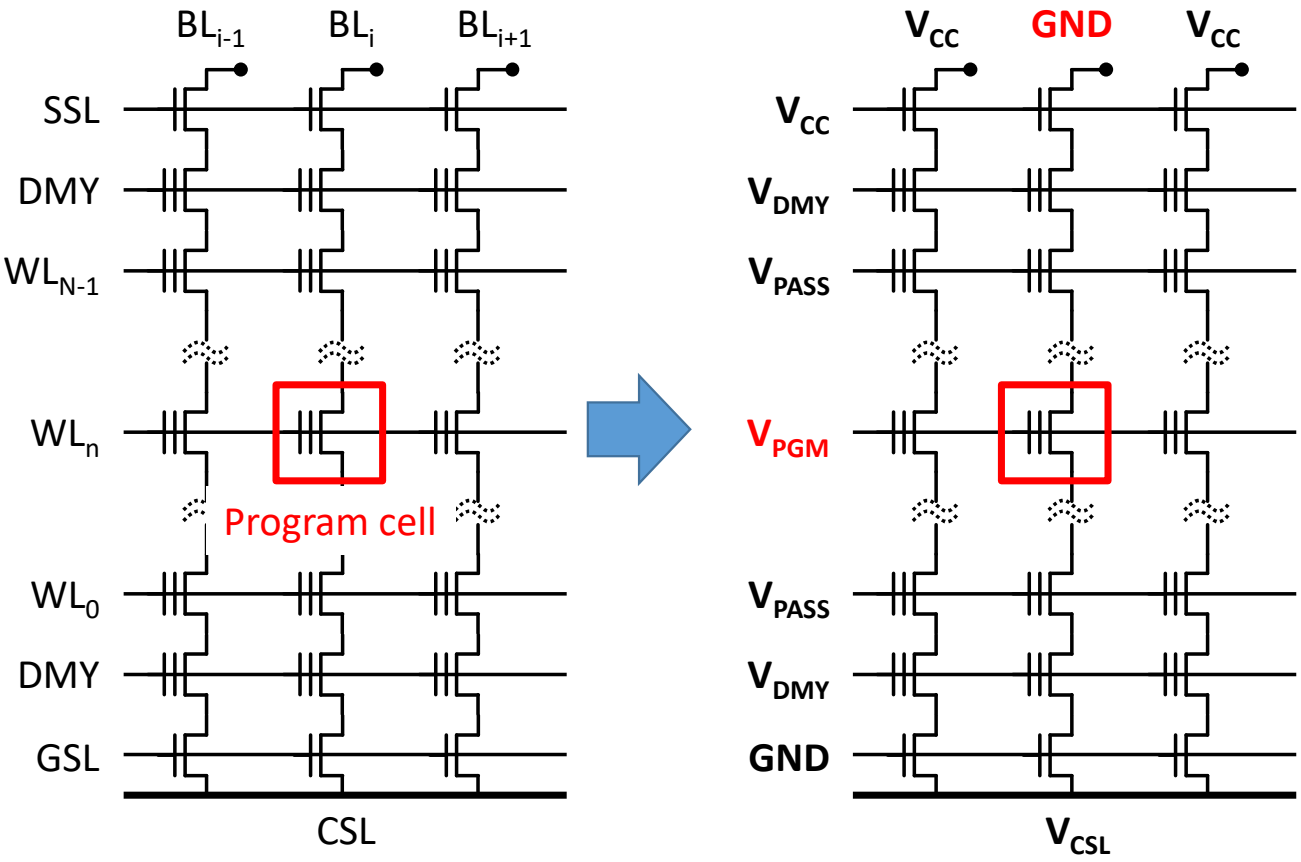


[2D FG Cell: Coupling ratio↑]



[3D CTF Cell: CR↑/Trap/High-κ]

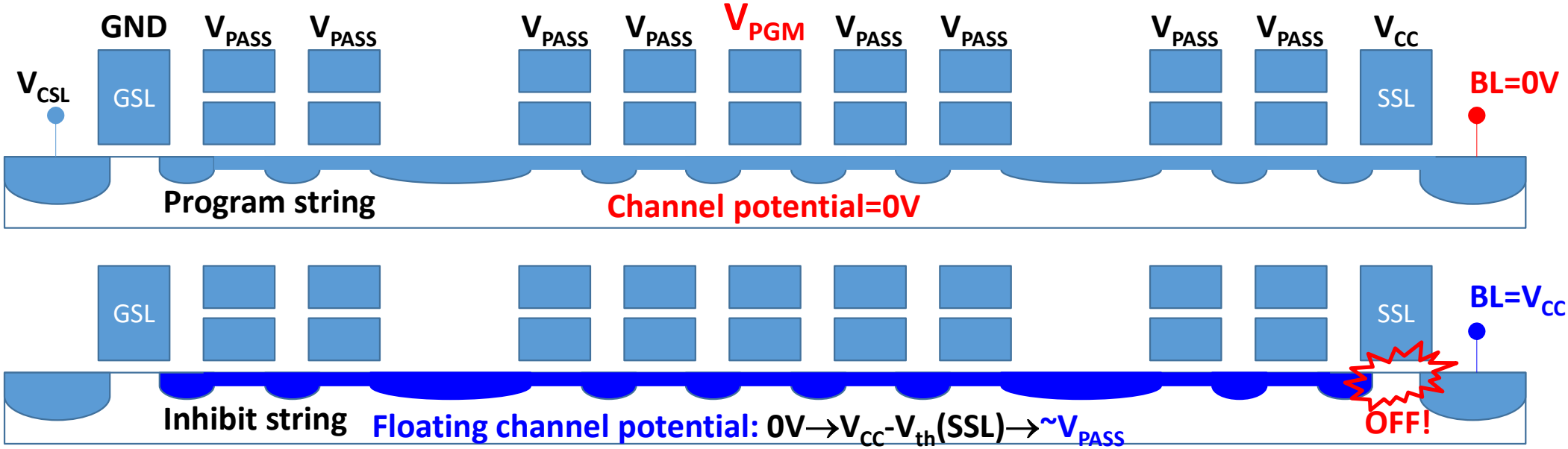
NAND Flash Memory – Basic Operation (Program)



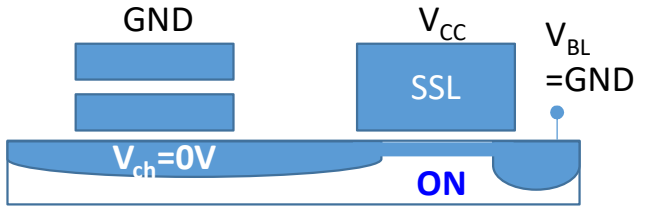
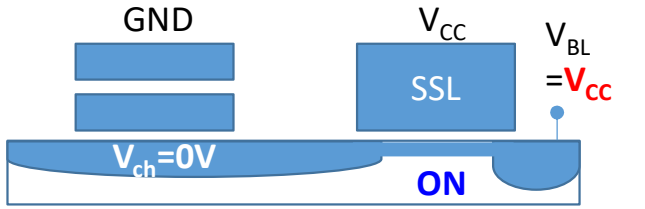
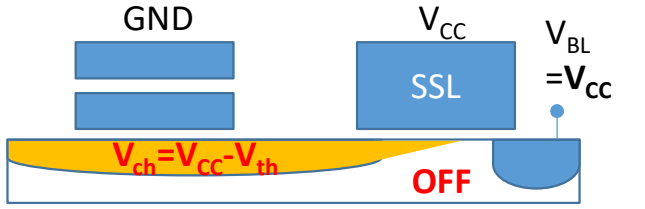
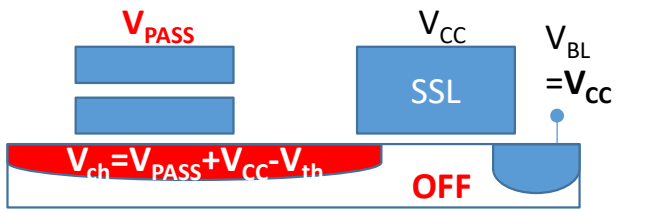
구성요소	인가전압
프로그램 WL	V_{PGM} (Max ~20V)
나머지 WL	V_{PASS} (5~8V)
DMY WL	V_{DMY} (GND~V_{PASS})
Select BL	GND
Unselect BL	V_{CC}
String Select Line	V_{CC}
Ground Select Line	GND
Common Source Line	V_{CSL} (~1.5V)

NAND Flash Memory – Basic Operation (Self-Boosting)

- WL에 V_{PGM}이 인가되어 있더라도, BL에 V_{CC}가 인가되면 program 안됨.
- BL에 V_{CC} 인가 시, channel의 전위가 높아지는 Self-boosting 현상 발생
- WL과 channel사이 전위차가 감소하여 program 되지 않음.



NAND Flash Memory – Basic Operation (Self-Boosting)

Step	V_{WL}	V_{SSL}	V_{BL}	V_{ch}	설명	Schematic
1	GND	V_{CC}	GND	GND	SSL Tr.이 켜져 있고, $V_{BL}=V_{ch}=0V$	
2	GND	V_{CC}	V_{CC}	GND	SSL이 saturation mode로 동작 Channel내 전자가 BL으로 이동 V_{ch}이 증가하기 시작	
3	GND	V_{CC}	V_{CC}	V_{CC}-V_{th}	Vch이 VCC-Vth까지 증가하면 SSL Tr.은 turn off 상태가 되고, channel은 floating 상태가 됨	
4	V_{PASS}	V_{CC}	V_{CC}	V_{PASS}+V_{CC}-V_{th}	Floating된 channel의 potential이 V_{PASS}에 의해 증가	

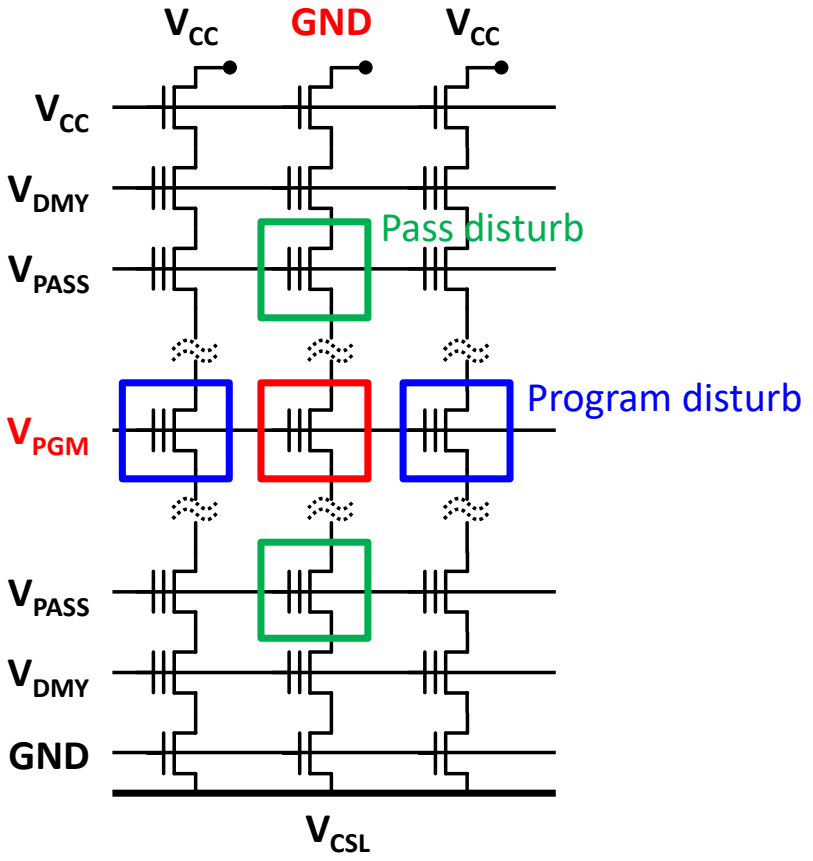
NAND Flash Memory – Basic Operation (Disturb)

- 어레이 내에서 프로그램이 되지 않기를 원하는 셀: Inhibit cell
- Inhibit cell이 soft program되는 현상

  : **Disturb**

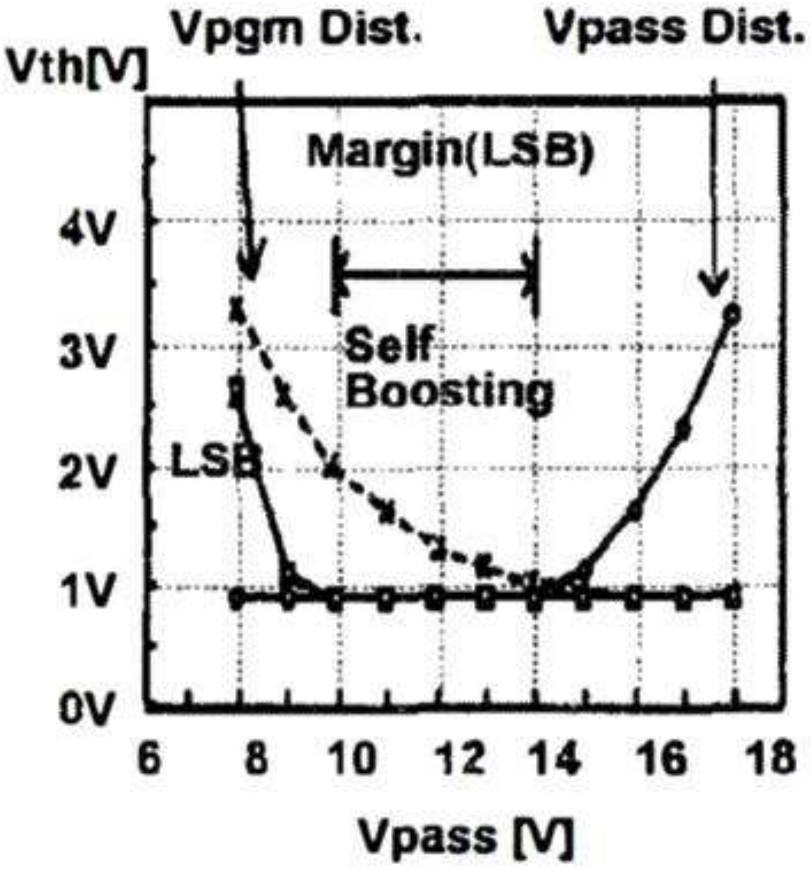
- 같은 String 내에 있는 Inhibit cell은 V_{PASS}에 의한 Pass disturb를 받음.

- 같은 WL을 공유하고 있는 Inhibit cell은 V_{PGM}-V_{ch}에 의한 Program disturb를 받음.

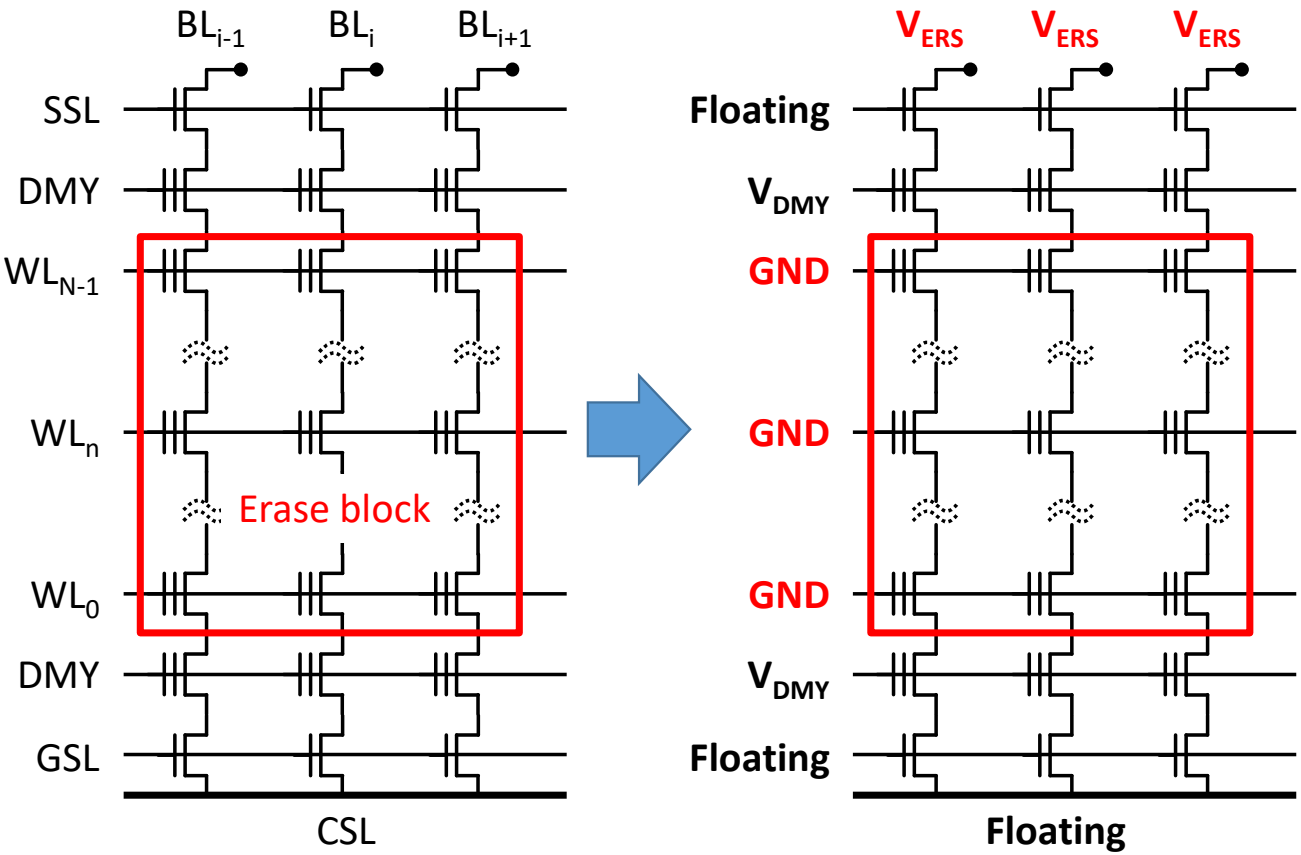


NAND Flash Memory – Basic Operation (Disturb)

- V_{PASS}를 낮추면 self-boosting된 string의 channel potential이 감소하여 program disturb가 나빠짐
- V_{PASS}를 높이면 V_{PASS}에 의한 soft program때문에 pass disturb가 나빠짐
- Program disturb와 pass disturb간의 trade-off를 고려하여 V_{PASS}를 결정함

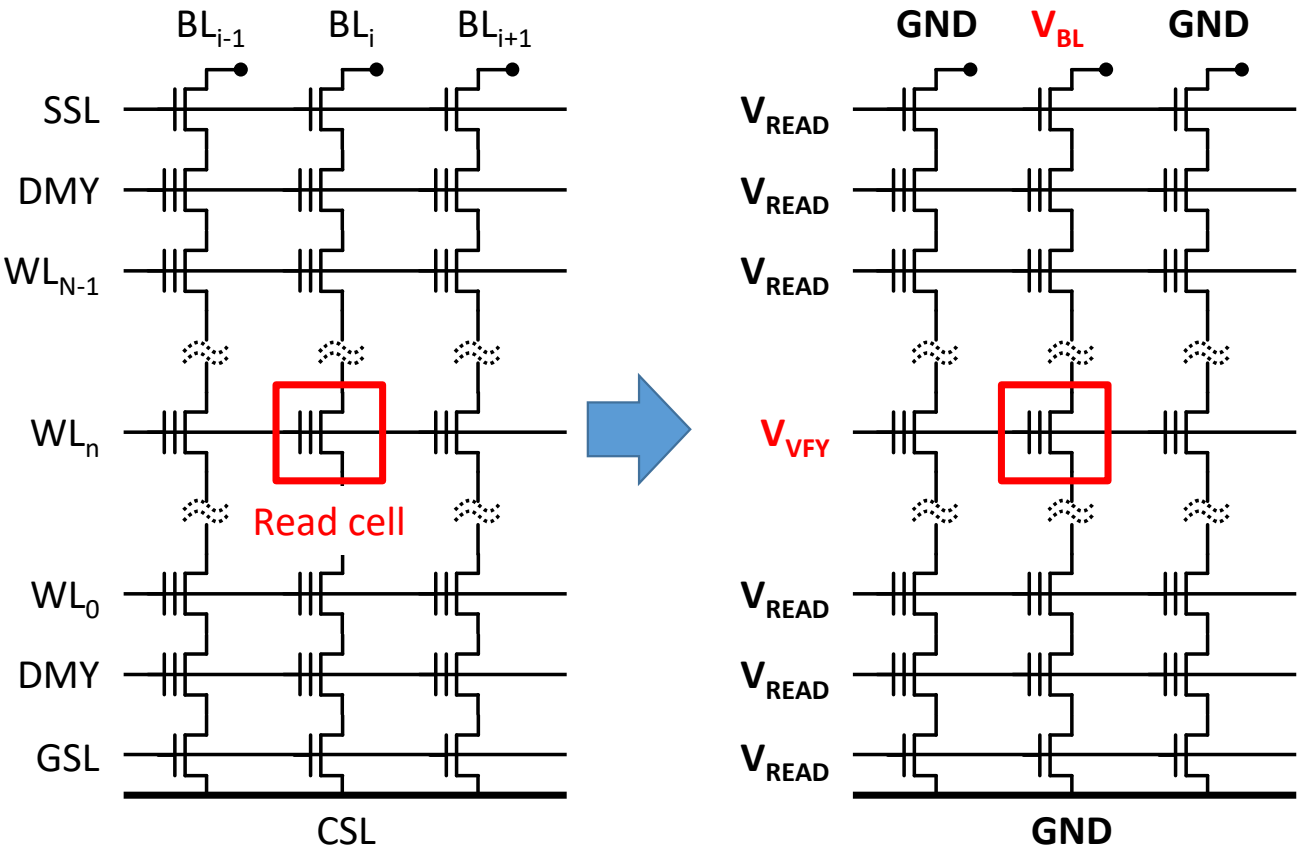


NAND Flash Memory – Basic Operation (Erase)



구성요소		인가전압
WL		GND
DMY WL		V_{DMY} (GND~V_{ERS})
2D	Bulk	V_{ERS}
	BL	Floating
3D	BL	V_{ERS}
String Select Line		Floating
Ground Select Line		Floating
Common Source Line		Floating

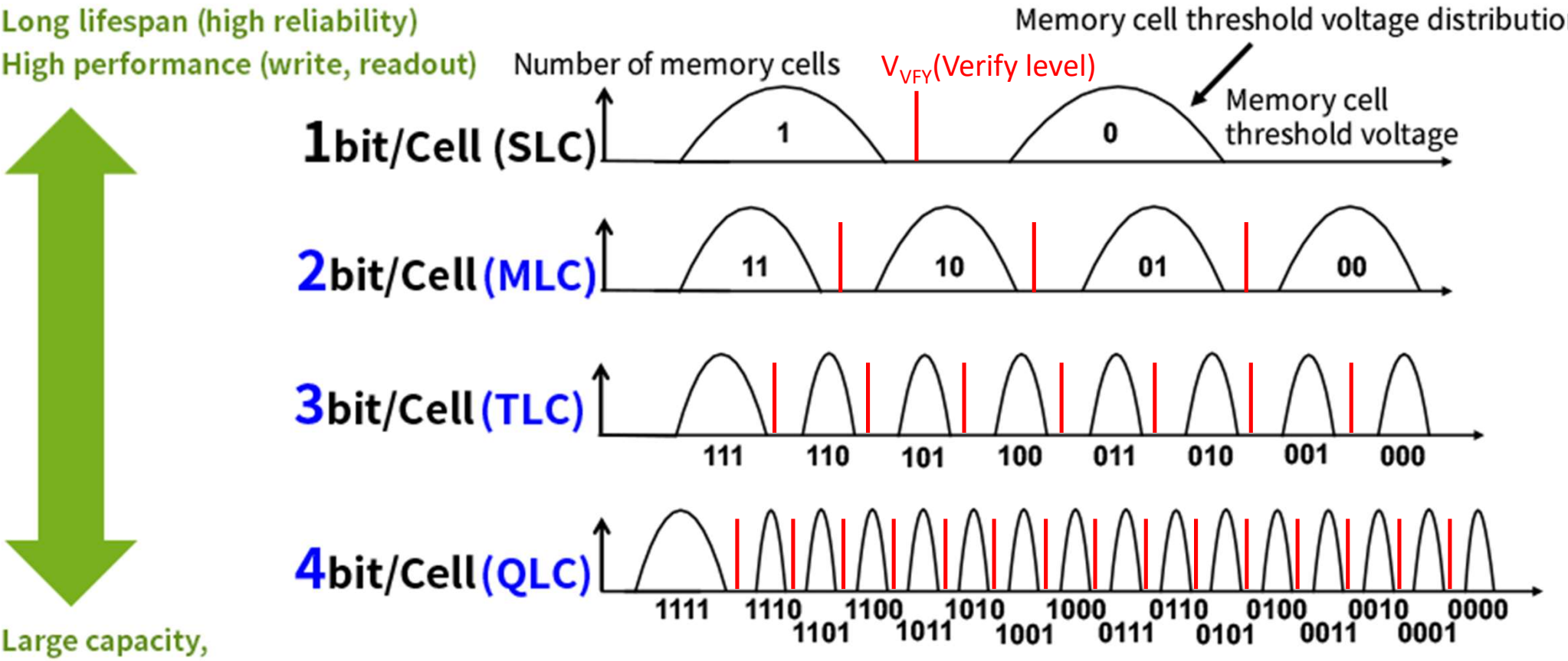
NAND Flash Memory – Basic Operation (Read)



구성요소	인가전압
Read WL	V_{VFY} (Verify level)
나머지 WL	V_{READ} (4~6V)
DMY WL	V_{READ}
Select BL	V_{BL} (~1V)
Unselect BL	GND
String Select Line	V_{READ}
Ground Select Line	V_{READ}
Common Source Line	GND

NAND Flash Memory – Multi-Level Cell

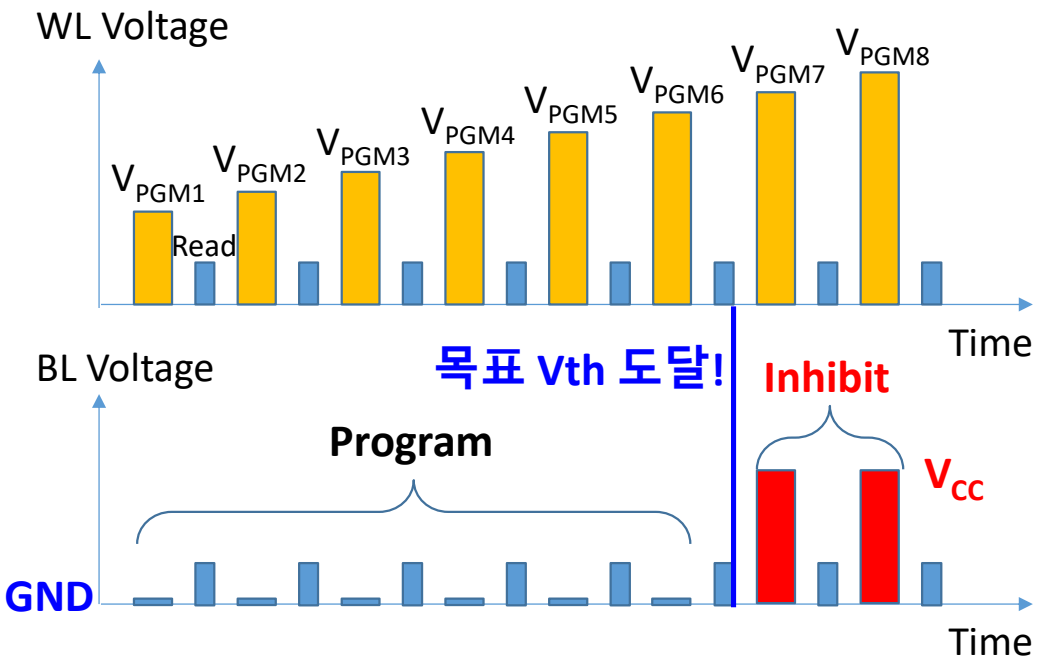
Long lifespan (high reliability)
High performance (write, readout)

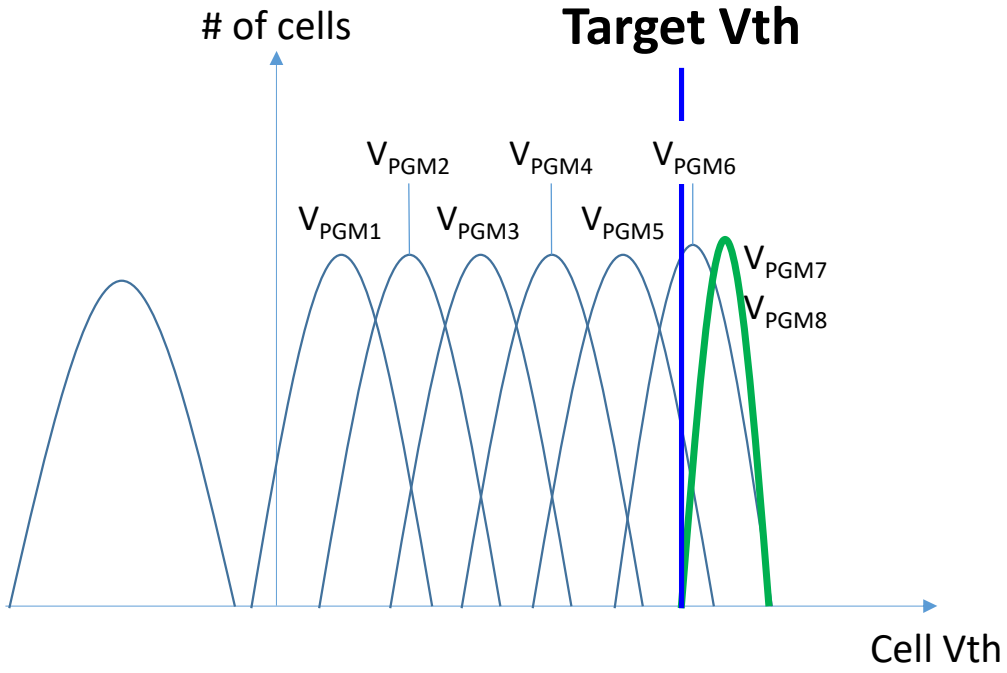


Large capacity,
low cost (cost per amount of data)

NAND Flash Memory – ISPP

- Cell Vth 산포 감소 위해 ISPP(Incremental Step Pulse Programming) 이용
- Program&Read를 반복하면서 목표 Vth에 도달하지 않은 cell만 program

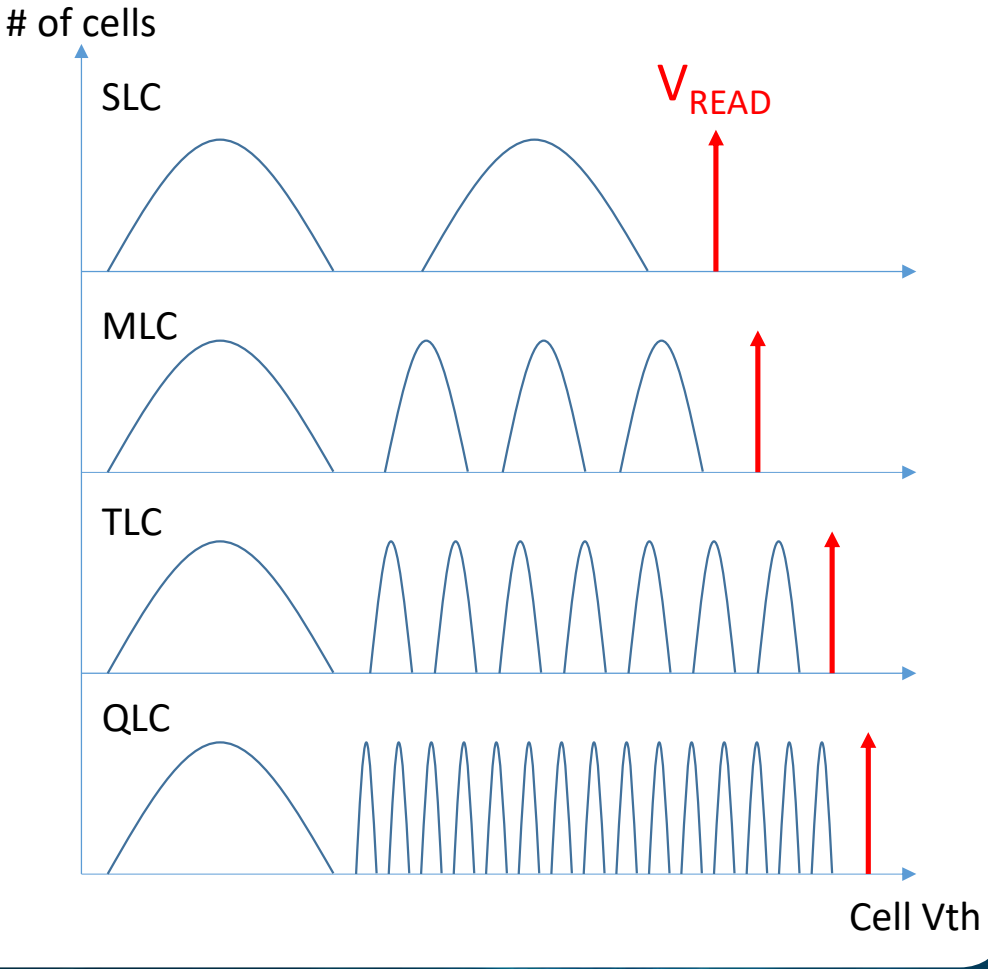




NAND Flash Memory – Read disturb

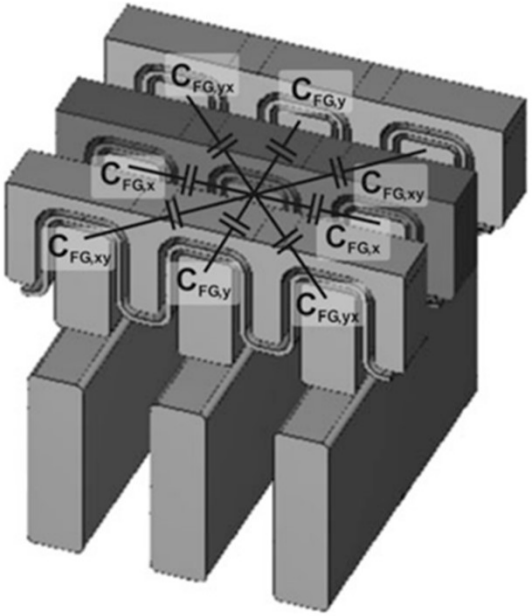
- MLC, TLC, QLC로 제품이 진화하면서 필요한 Vth window가 증가하고 있고, 더 높은 V_{READ}가 필요해지고 있음

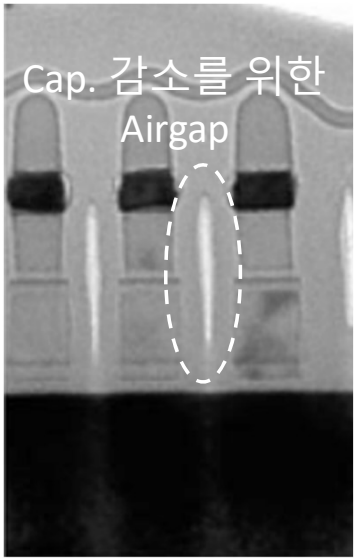
- Pass disturb와 마찬가지로, read 동작을 반복적으로 진행하면 V_{READ}에 의한 soft program이 발생하고 이를 read disturb라고 함

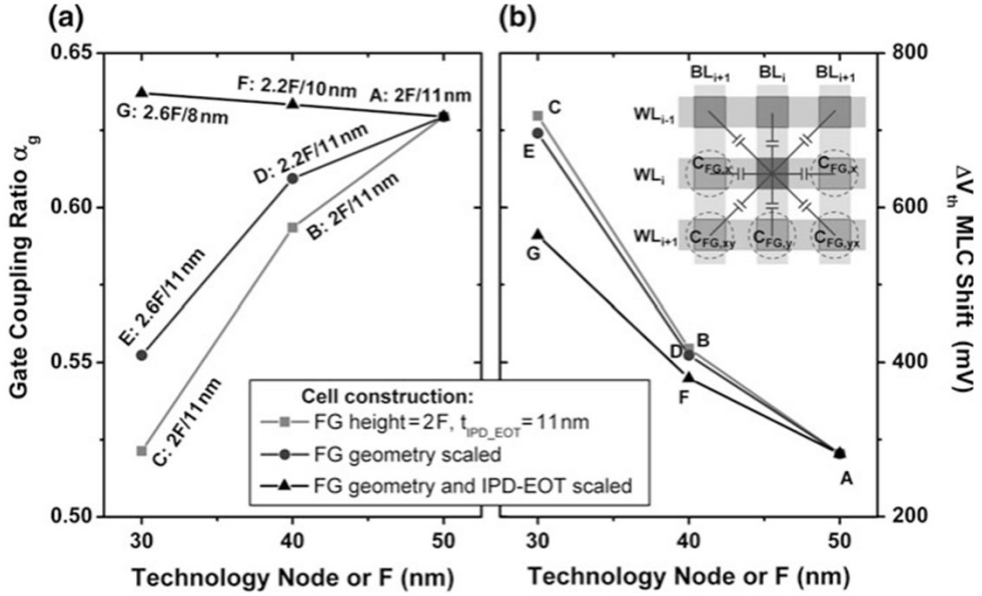


NAND Flash Memory – Interference

- 인접한 cell의 Vth가 증가함에 영향을 받아서 Vth가 같이 증가하는 현상을 interference라고 하고, 소자가 작아질수록 그 영향이 증가함
- Cell Vth 산포의 upper tail을 증가시키는 중요한 원인 중 하나임

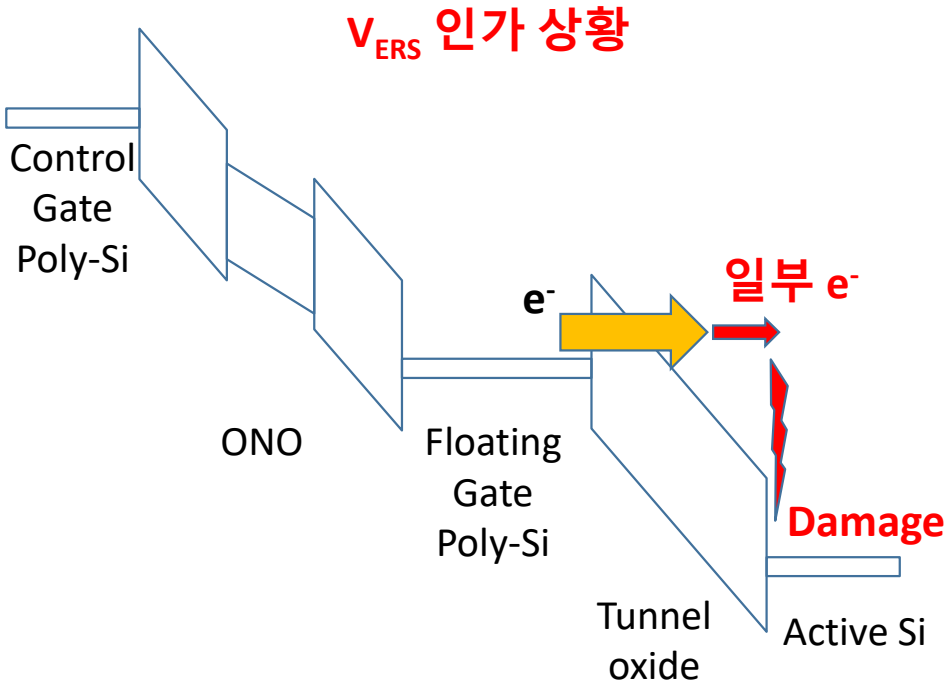


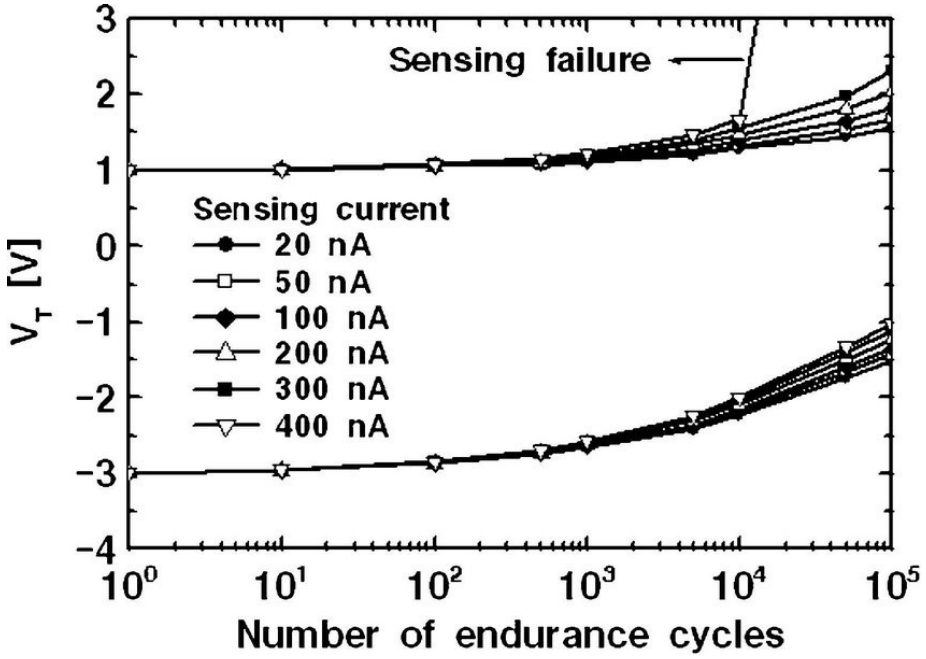




NAND Flash Memory – Reliability (Endurance)

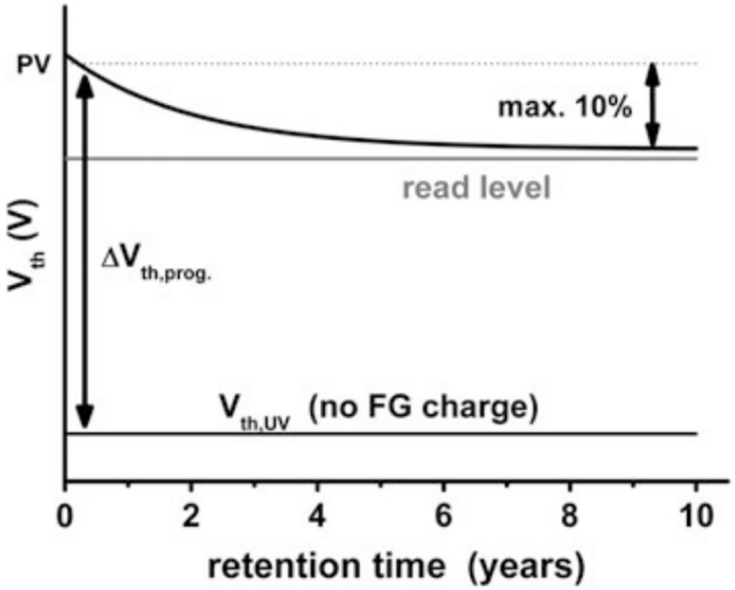
- 반복된 program/erase 동작에 의해 tunnel/blocking layer가 damage를 받음
- Si-SiO_2에 생성된 defect에 의해 transistor의 Vth 증가 및 전류 감소

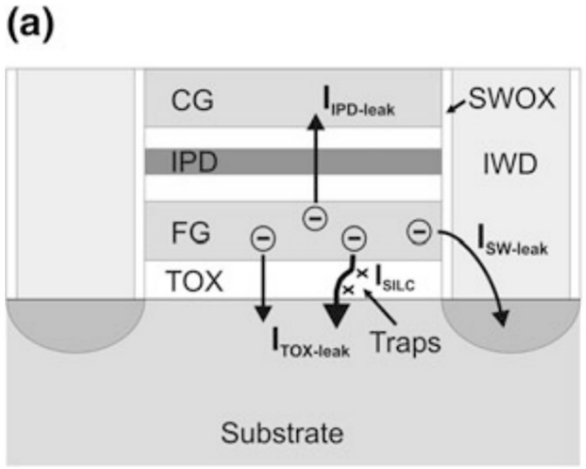


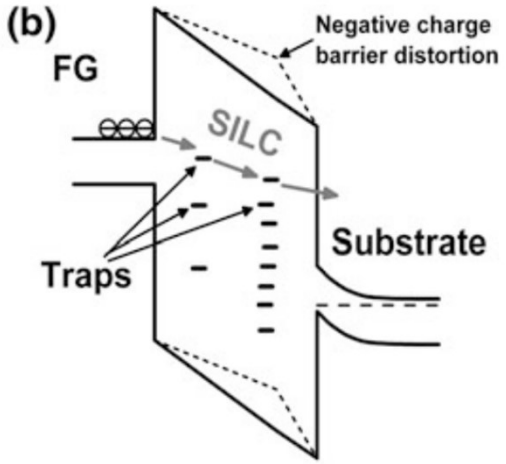


NAND Flash Memory – Reliability (Retention)

- 저장된 전하가 tunnel/blocking layer를 통해 active/gate로 빠져나가 transistor의 Vth가 감소하는 현상 발생함
- Cell Vth 산포의 lower tail를 만드는 주요 원인임



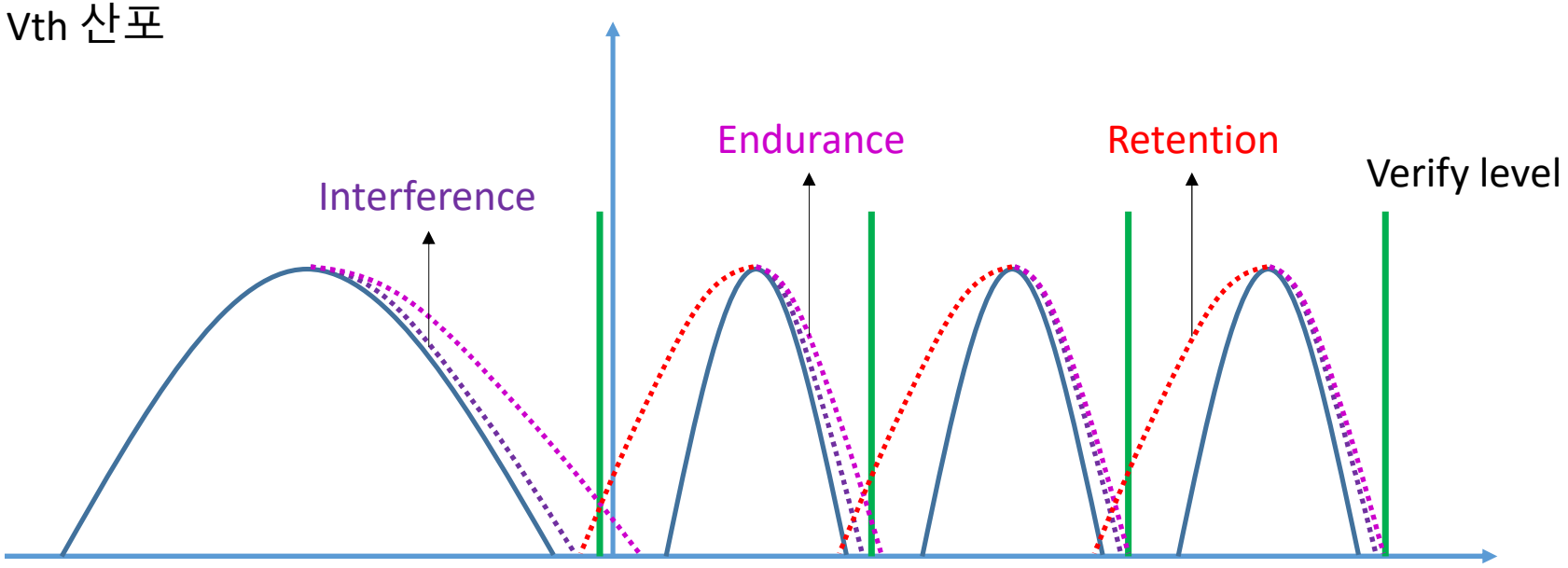




NAND Flash Memory – Reliability (Vth distribution)

- Endurance와 retention이 cell Vth distribution에 미치는 영향

MLC Cell Vth 산포

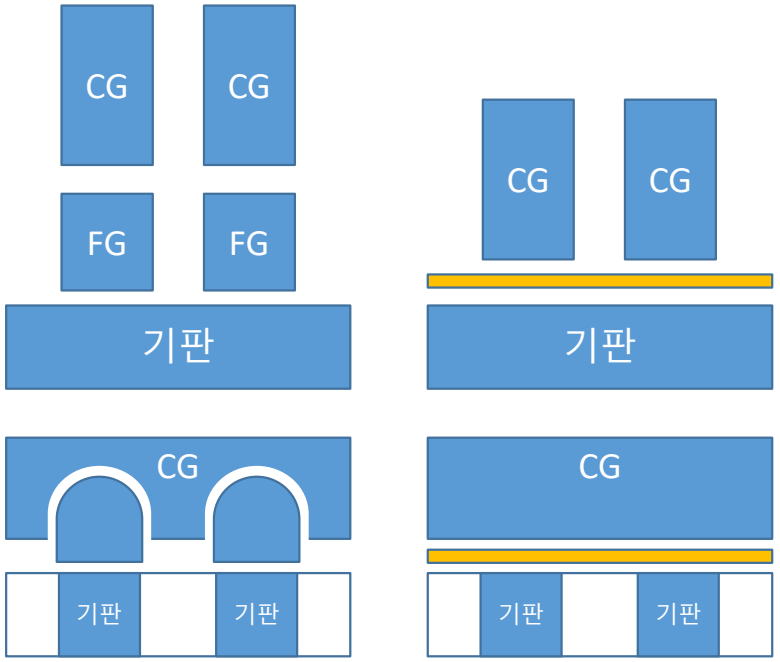


Summary and FG vs. CTF

- CTF는 FG 대비 WL간 interference, endurance 등에서 우수함
- 무엇보다 3D integration에 적합한 단순한 구조가 가장 큰 장점

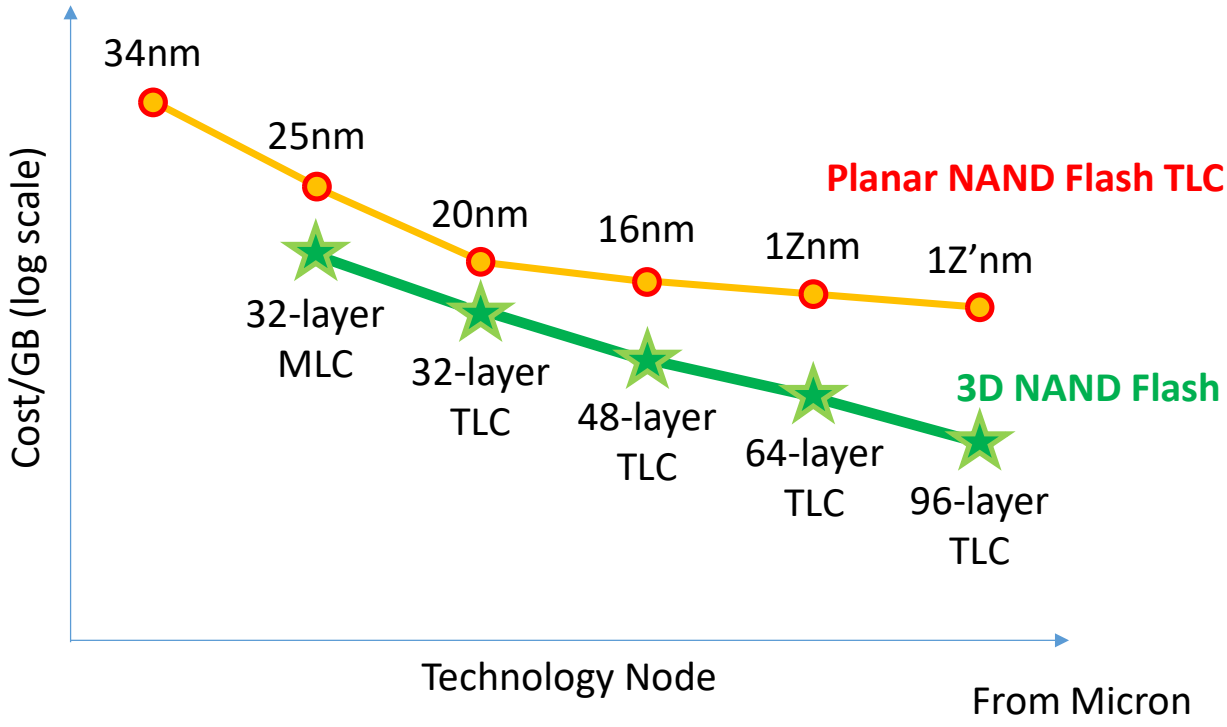
항목	설명	FG	CTF
Program	쓰기 동작, Cell V_{th}↑	**Good**	Fair
Erase	지우기 동작, Cell V_{th}↓	**Good**	Fair
Read	Cell V_{th} 읽기 동작	Fair	Fair
Disturb	V_{PGM}, V_{PASS}, V_{READ}에 의해 발생하는, 원치 않는 V_{th} 변동 현상	Fair	Fair
Interference	인접한 cell의 V_{th} 변화에 의한 원치 않는 V_{th} 변동 현상	**Poor**	**Good**
Endurance	반복된 Program/Erase에 의한 소자 특성 열화	**Poor**	**Good**
Retention	저장된 전하의 소실에 의한 V_{th} 변화	**Good***	**Poor***

*Storage layer에 있는 전하가 전부 빠져버리는 total charge loss 현상이 없다는 측면에서는 CTF가 FG 대비 유리함

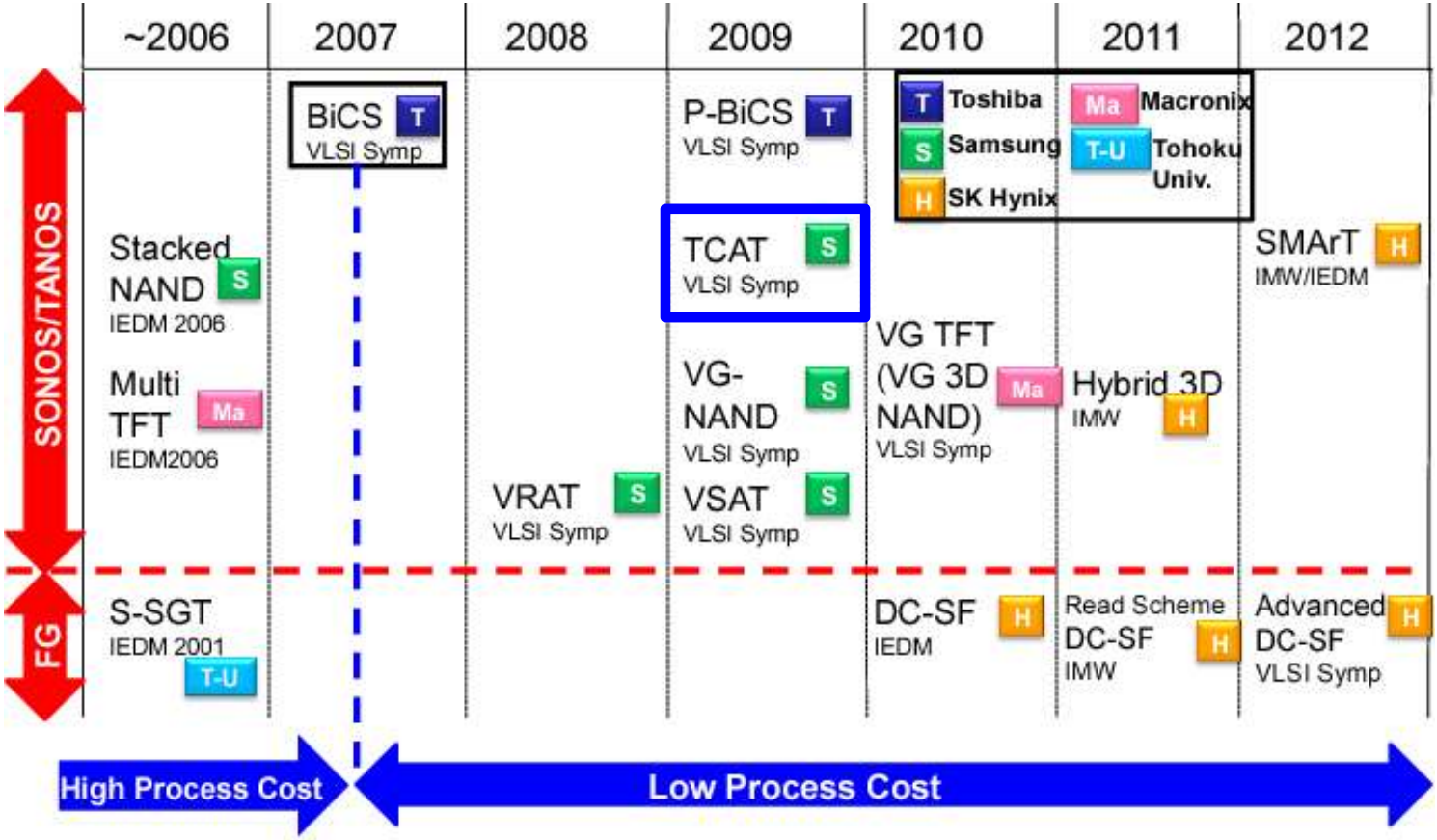


Introduction of 3D NAND Flash Memory

- 지속적인 가격경쟁력 확보를 위해 2D→3D로의 전환이 필수



Introduction of 3D NAND Flash Memory



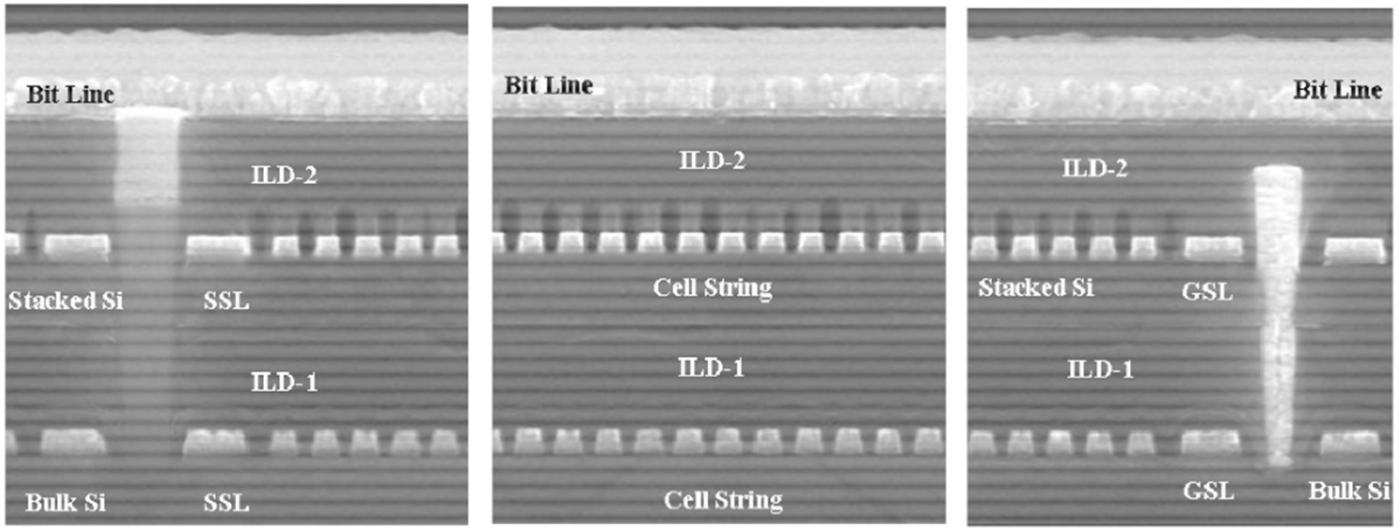
3D NAND – Stacked NAND (IEDM 2006)

Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node

Soon -Moon Jung, Jaehoon Jang, Wonseok Cho, Hoosung Cho, Jaehun Jeong, Youngchul Chang, Jonghyuk Kim
Youngseop Rah, Yangsoo Son, Junbeom Park, Min-Sung Song, Kyoung-Hon Kim, Jin-Soo Lim and Kinam Kim

R&D Center, Samsung Electronics

Planar CTF 적층
비용 측면 비효율적

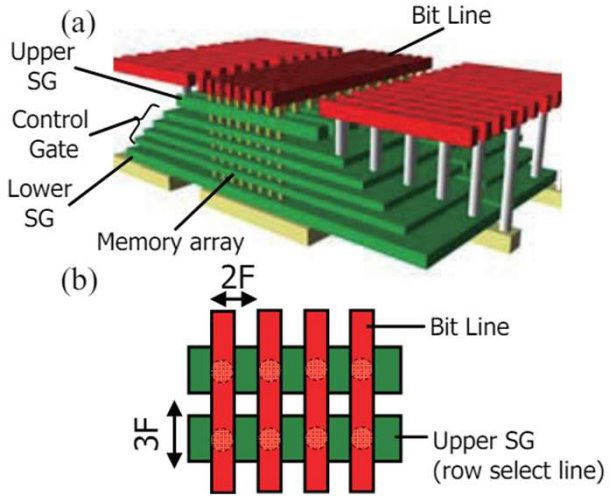


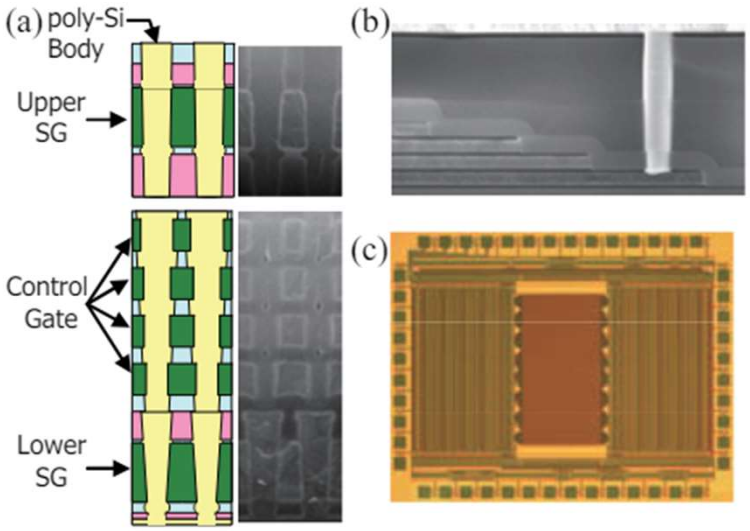
3D NAND – BiCS (VLSI Tech. 2007)

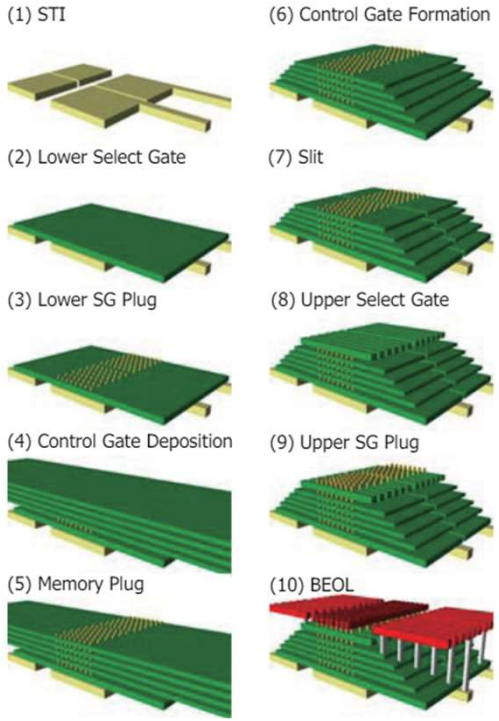
Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

H.Tanaka, M.Kido, K.Yahashi*, M.Oomura*, R.Katsumata, M.Kito, Y.Fukuzumi, M.Sato, Y.Nagata**
Y.Matsuoka, Y.Iwata, H.Aochi and A.Nitayama
Center for Semiconductor Research & Development and Process & Manufacturing Engineering Center*,
TOSHIBA Corporation, Semiconductor Company
Toshiba Information Systems (Japan) Corporation**

최초의 3D NAND prototype
Poly-Si gate 기반 → 특성 열세





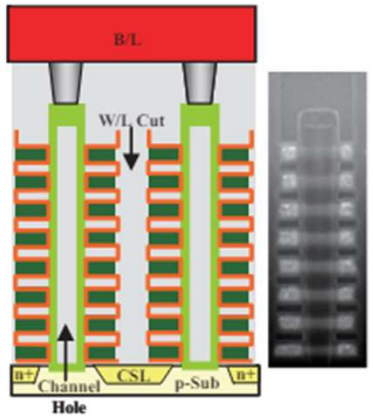


3D NAND – TCAT (VLSI Tech. 2009)

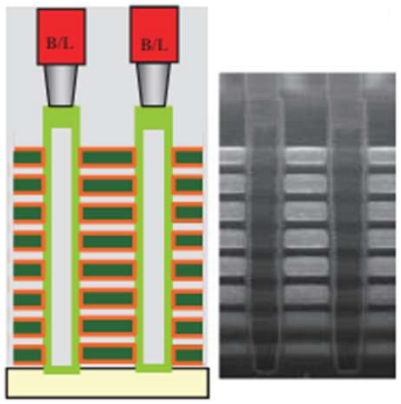
Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

Jaehoon Jang, Han-Soo Kim, Wonseok Cho, Hoosung Cho, Jinho Kim, Sun Il Shim, Younggoan Jang, Jae-Hun Jeong, Byoung-Keun Son, Dong Woo Kim, Kihyun Kim, Jae-Joo Shim, Jin Soo Lim, Kyoung-Hoon Kim, Su Youn Yi, Ju-Young Lim, Dewill Chung, Hui-Chang Moon, Sungmin Hwang, Jong-Wook Lee*, Yong-Hoon Son*, U-In Chung* and Won-Seong Lee
Advanced Technology Development Team 2&Process Development Team*, Memory R&D Center, Memory Division, Samsung Electronics Co. Ltd.,

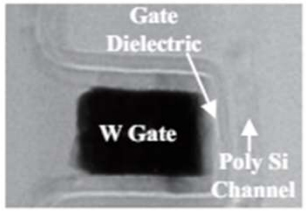
Metal gate 기반 → 특성 우세
WL replacement 공정 난이도↑



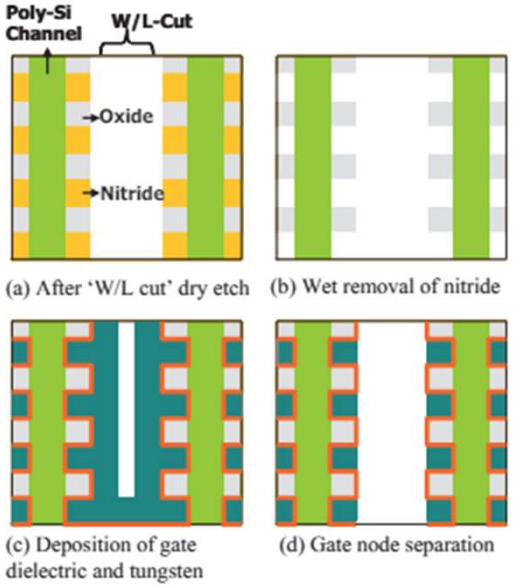
(a) X-Direction



(b) Y-Direction



(c) Cell



(a) After 'W/L cut' dry etch
(b) Wet removal of nitride
(c) Deposition of gate dielectric and tungsten
(d) Gate node separation

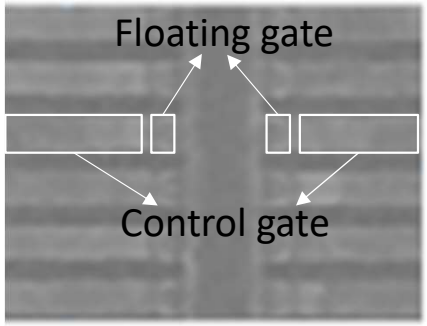
3D NAND – Floating gate 3D NAND CUA (IEDM 2015)

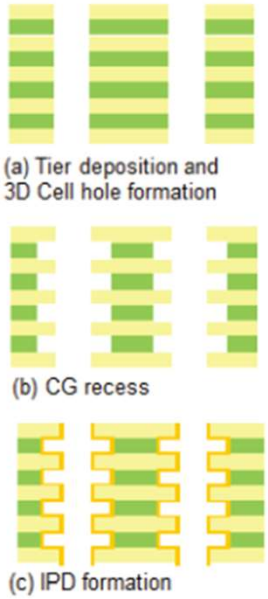
A Floating Gate Based 3D NAND Technology With CMOS Under Array

FG 3D NAND → 공정 복잡도 ↑
CMOS under Array→ Chip 면적↓

Invited Paper
Krishna Parat, Chuck Dennison‡
Intel Corporation, 2200 Mission College Blvd., Santa Clara, CA 95054 krishna.parat@intel.com
‡ Micron Technology,


(a)





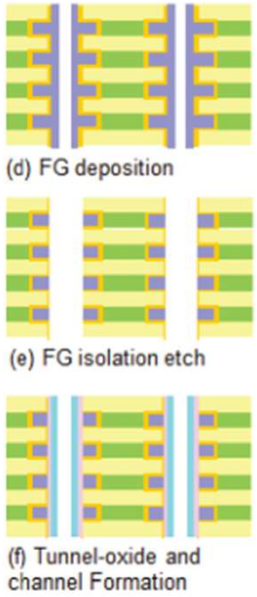
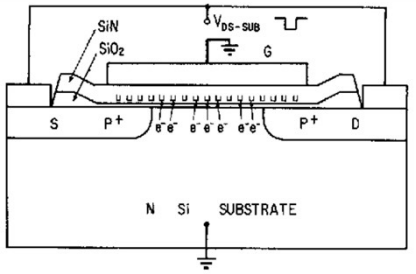
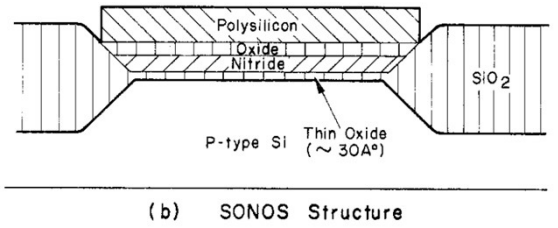
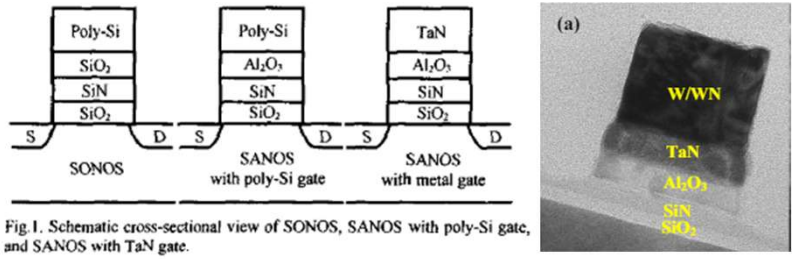


Figure 15. Die photo of the 3D 256Gb 2bits/cell & 384Gb 3bits/cell die with the CMOS decoder and sense amp circuits placed under the NAND array.

Evolution of CTF NAND Flash

소자 구조	설명	Schematic
MNOS (1967) Metal Nitride/Oxide Silicon	두꺼운 Nitride layer에 전자를 저장하는 메모리 소자	
SONOS (1977) Silicon Oxide/Nitride/Oxide Silicon	Poly-Si gate와 ONO sandwich 구조를 가지는 기본적인 CTF 구조 **Erase시 gate에서 trap layer로 전자가 넘어와서 erase가 잘 되지 않음**	 (b) SONOS Structure
TANOS (2003) TaN metal AlO/Nitride/Oxide Silicon	**Erase 특성 개선을 위해 High-κ/Metal gate를 적용**한 CTF 구조	 Fig.1. Schematic cross-sectional view of SONOS, SANOS with poly-Si gate, and SANOS with TaN gate.

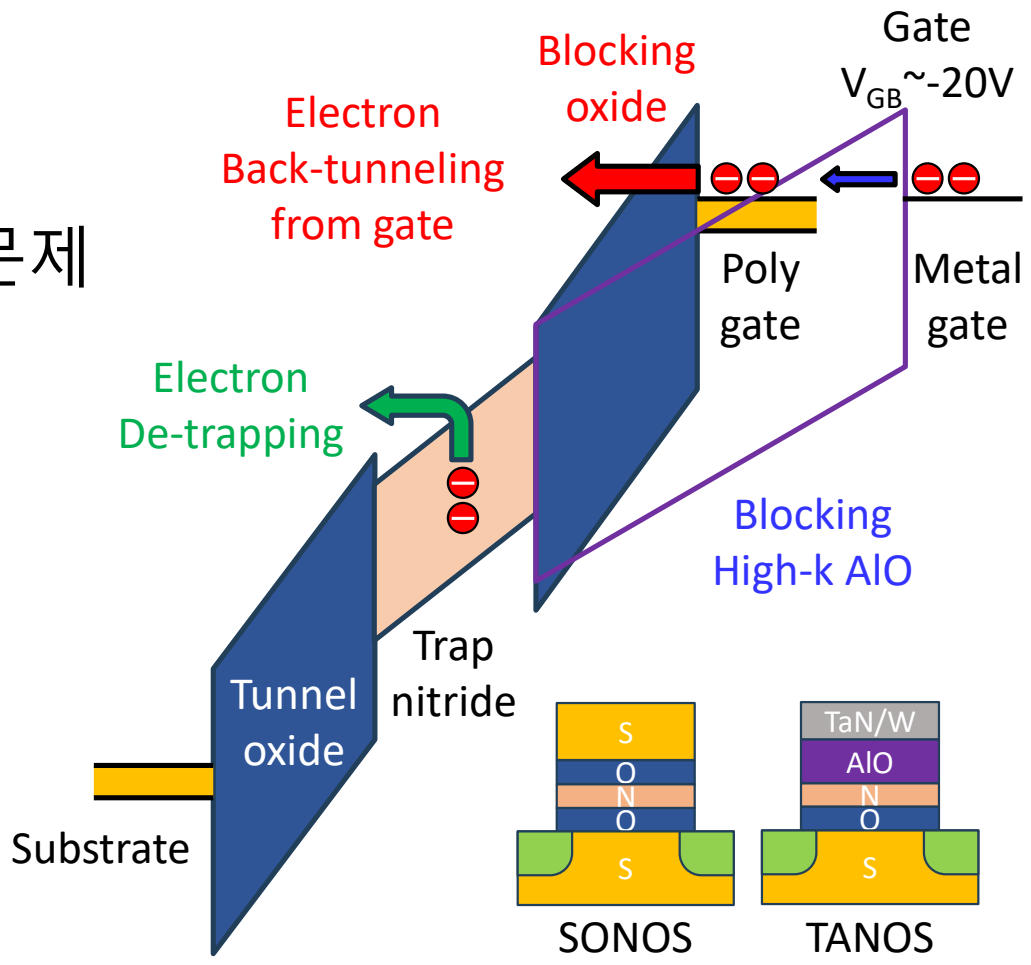
BiCS vs. TCAT

- BiCS는 SONOS 기반

→ Erase 특성 열세 및 WL 저항 증가 문제

- TCAT은 TANOS 기반

→ Erase 및 WL 저항 측면 유리하여 3D NAND reference로 자리 잡음



3D NAND Flash Memory – Architecture

- 각 층별 WL/GSL은 모두 하나로 묶여 있음 (Block별로는 분리됨)
- 같은 층에서 하나의 string을 선택하기 위해, SSL이 분리되어 있음

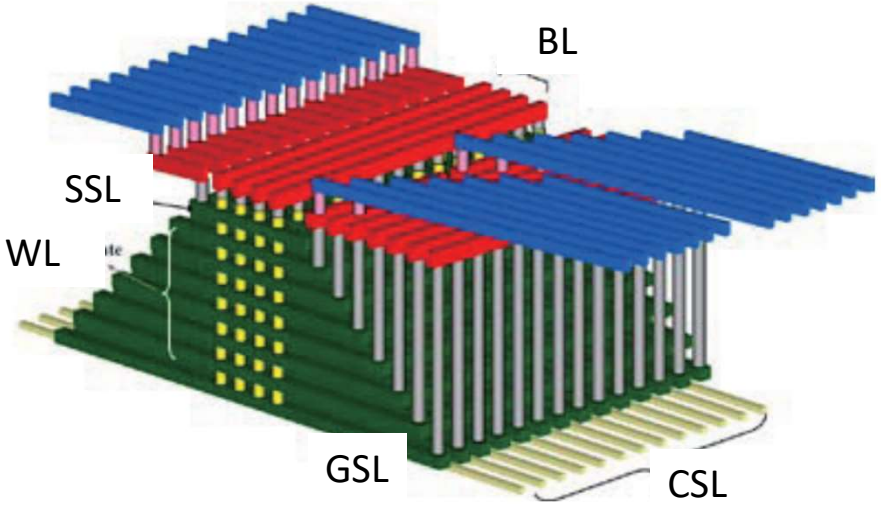
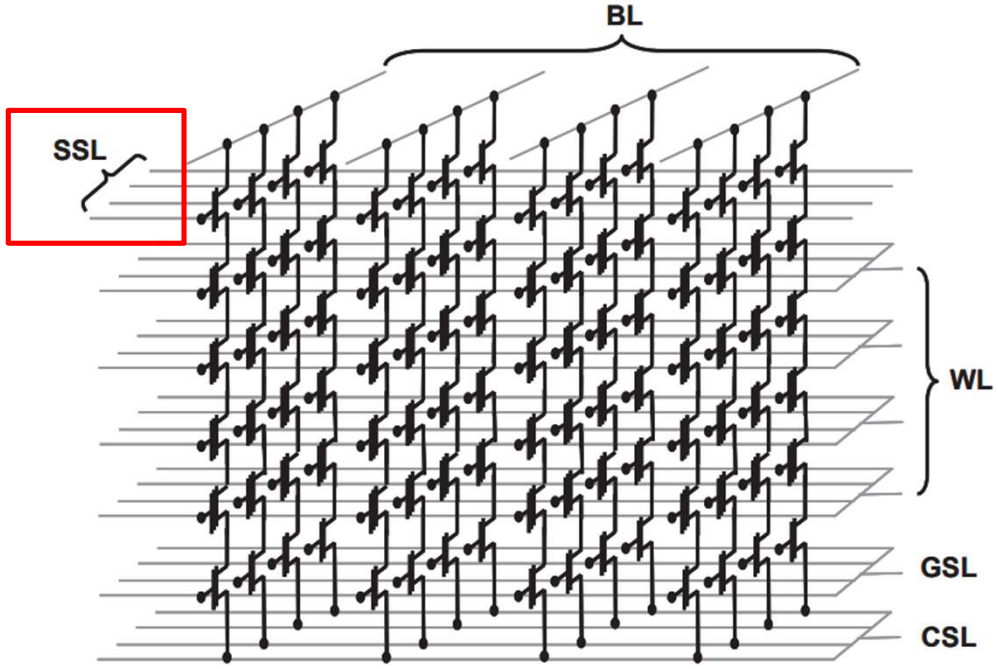
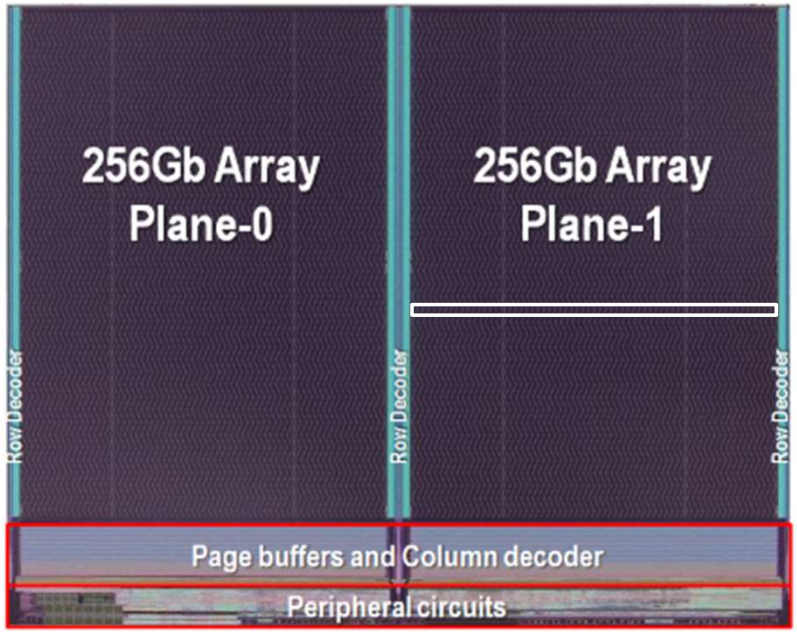


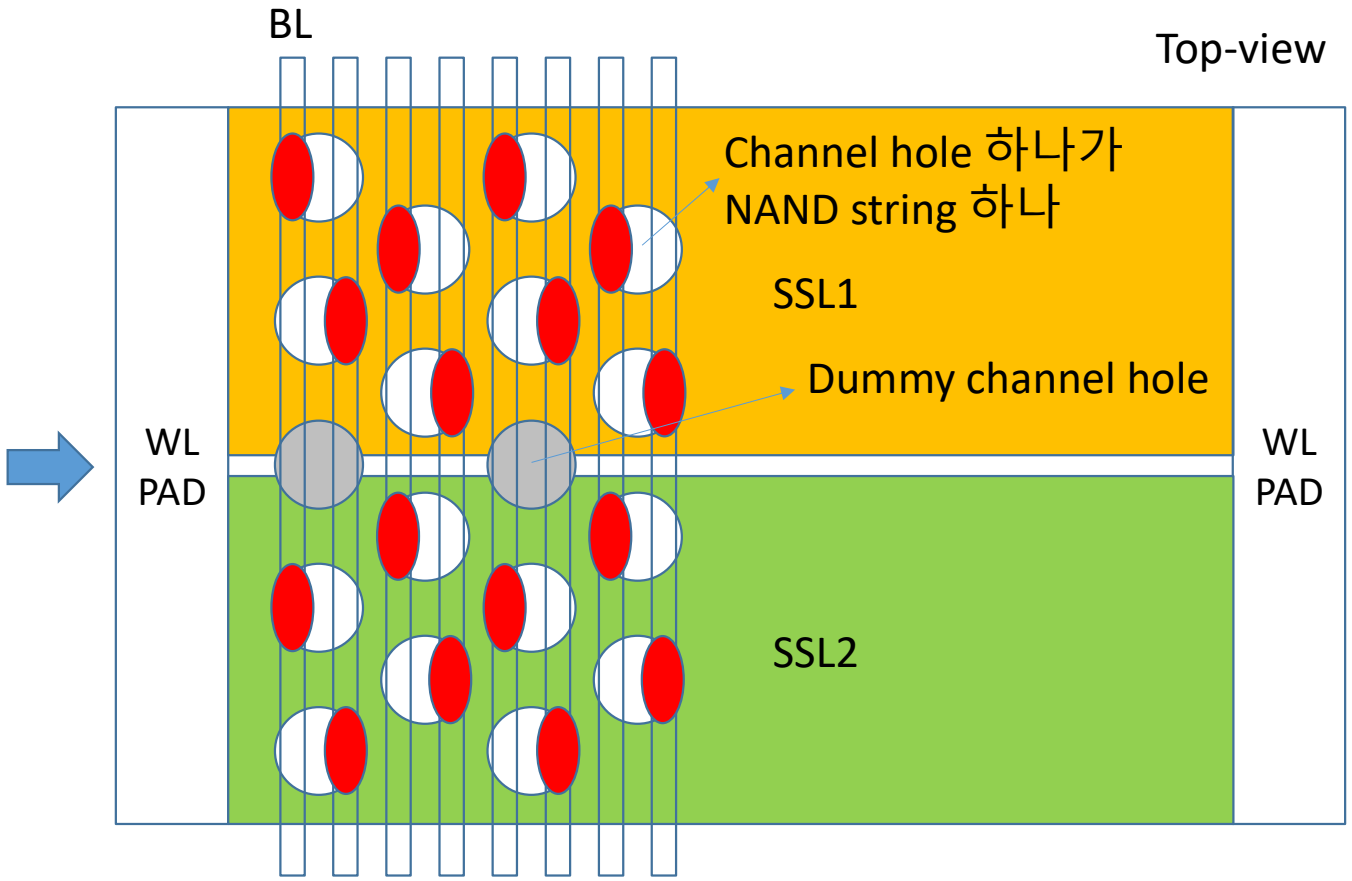
Fig.1 Birds-eye view of TCAT flash memory.



3D NAND Flash Memory – Chip architecture

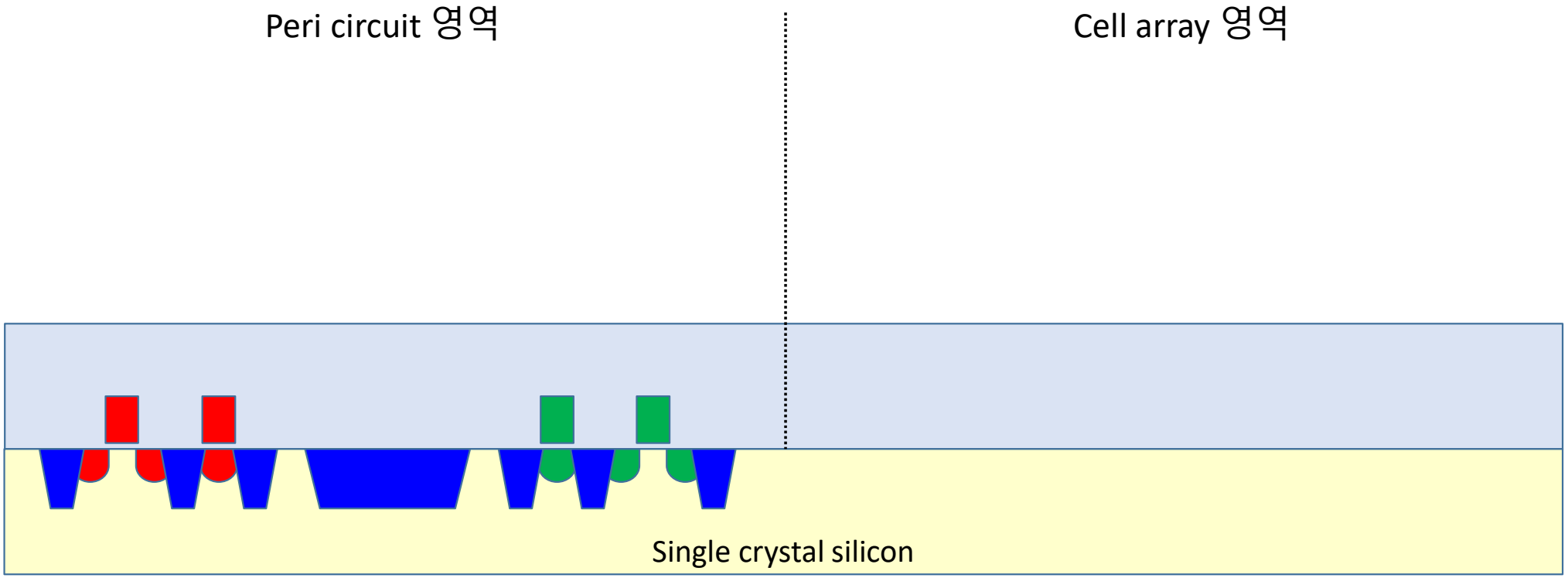


[Samsung's 64-layer 3D NAND in 2017]



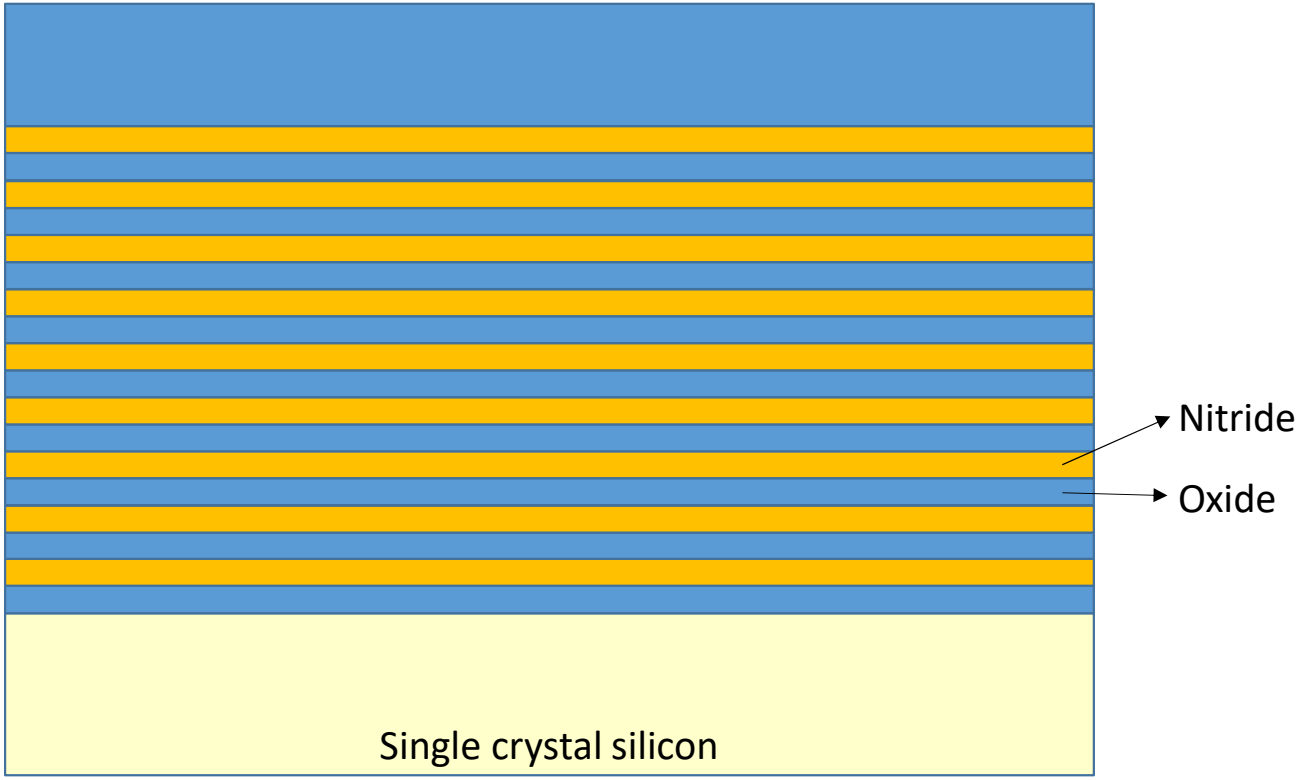
3D NAND Flash Memory – Process Integration

- 1. CMOS circuit fabrication



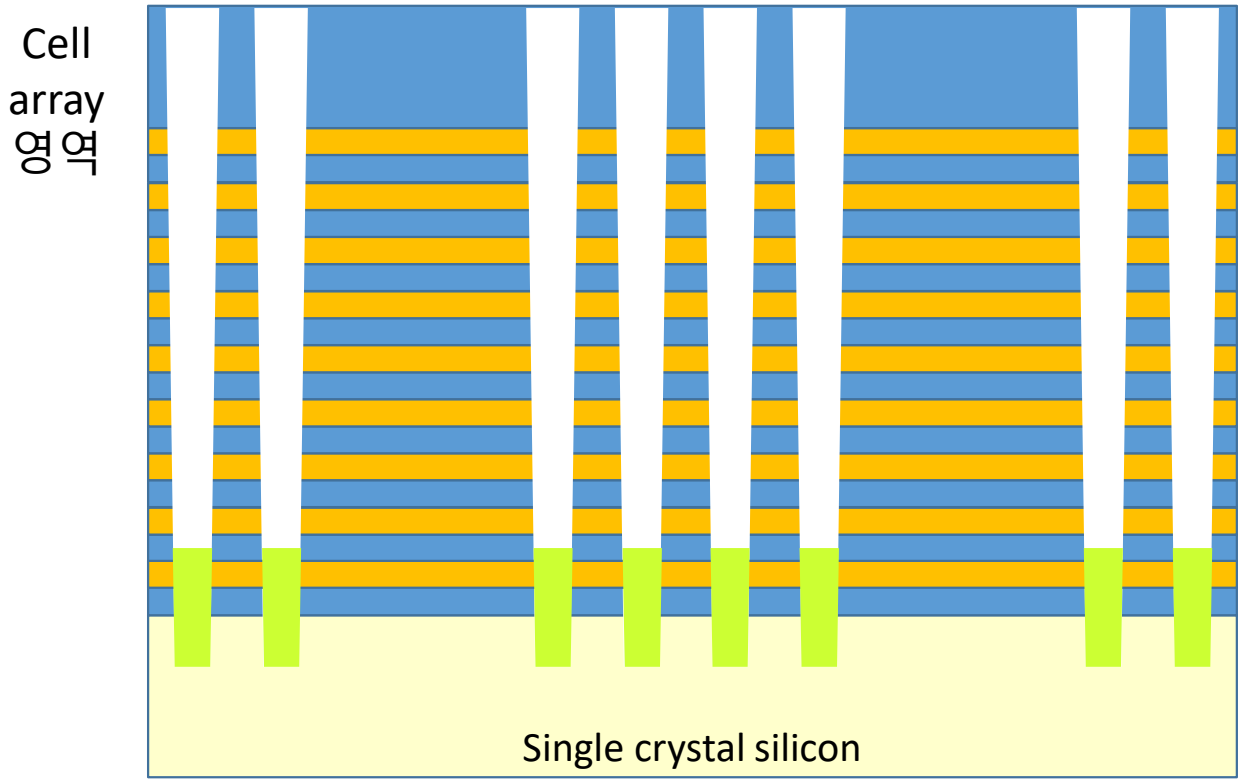
3D NAND Flash Memory – Process Integration

- 2. Oxide-Nitride mold 반복 형성



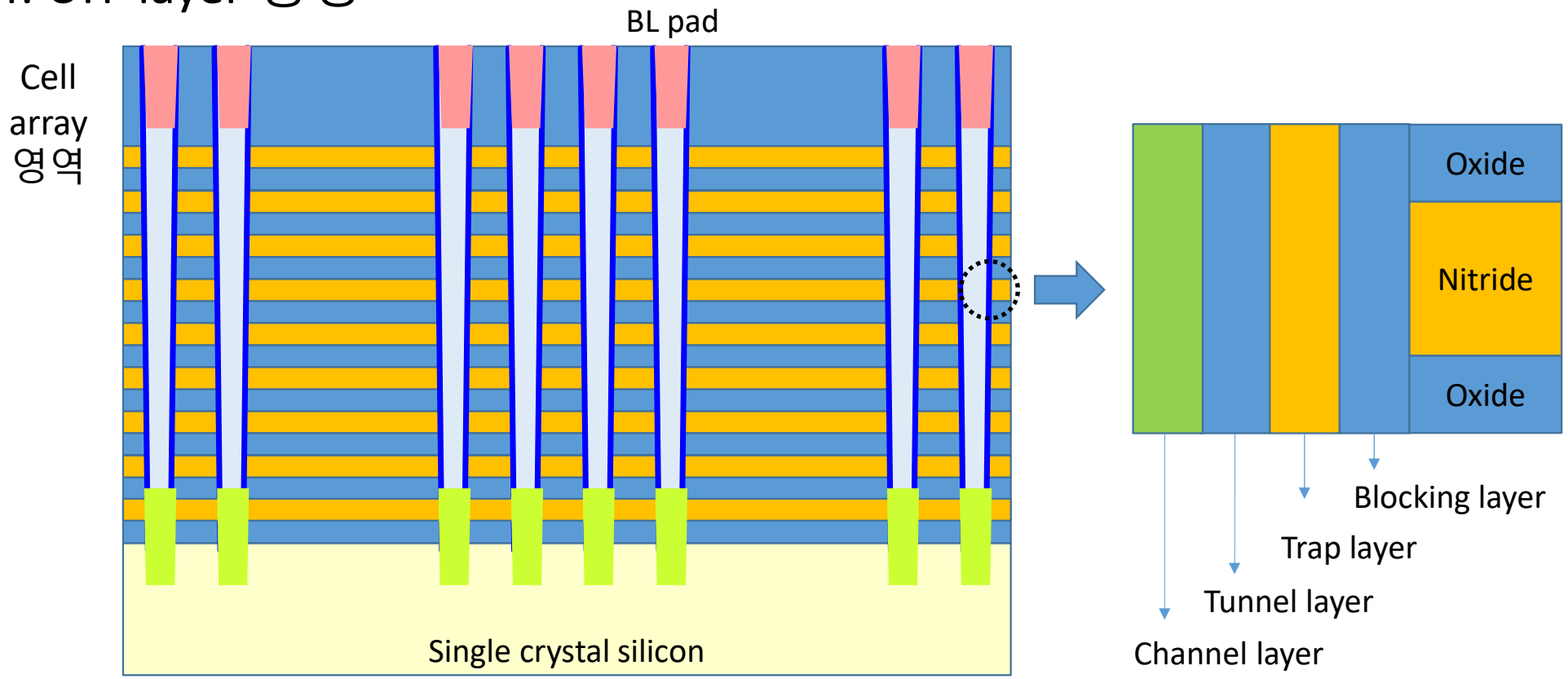
3D NAND Flash Memory – Process Integration

- 3. Channel hole etch



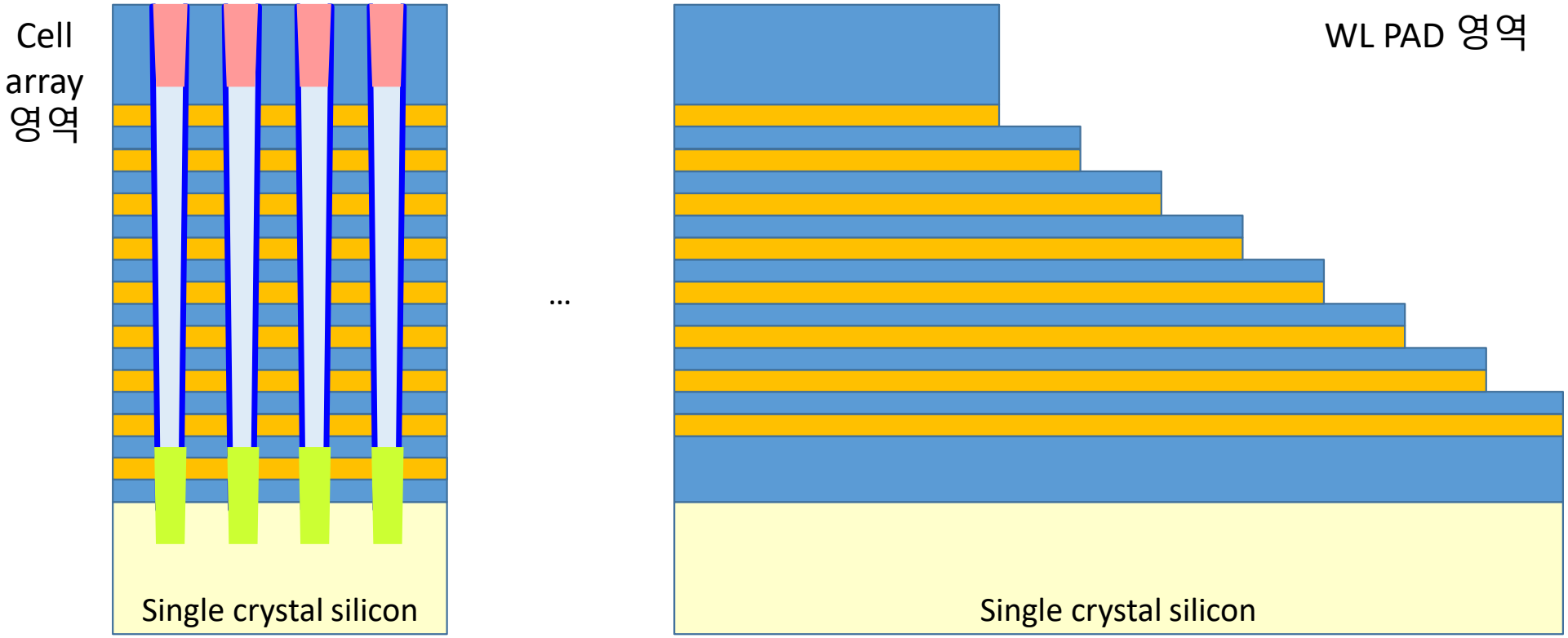
3D NAND Flash Memory – Process Integration

- 4. CTF layer 형성



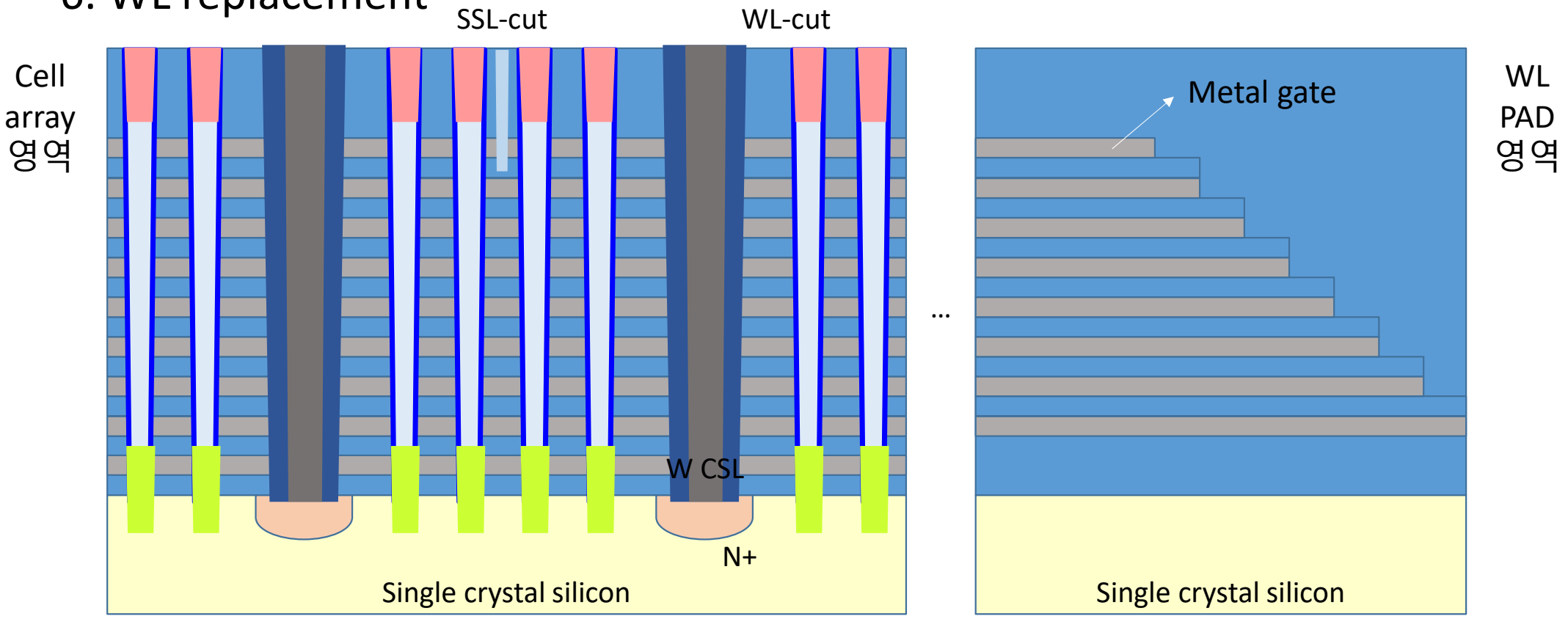
3D NAND Flash Memory – Process Integration

- 5. WL pad 형성



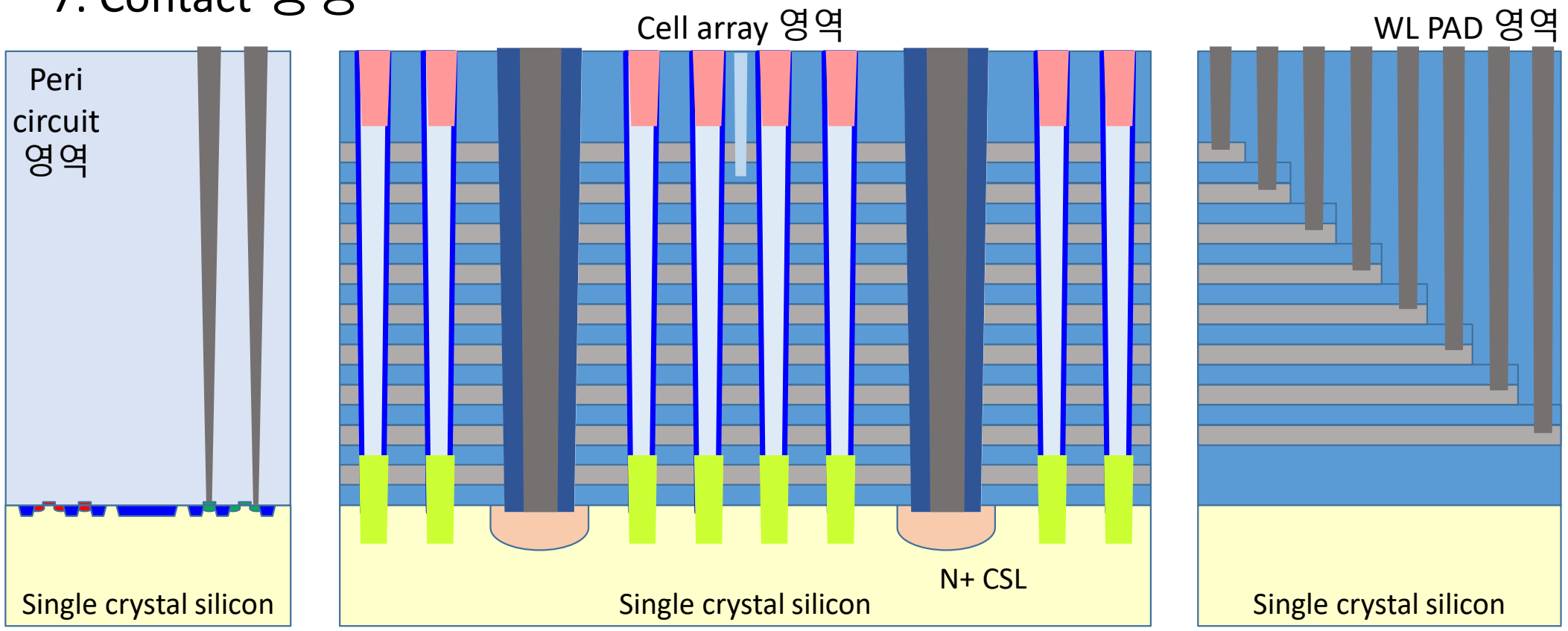
3D NAND Flash Memory – Process Integration

- 6. WL replacement

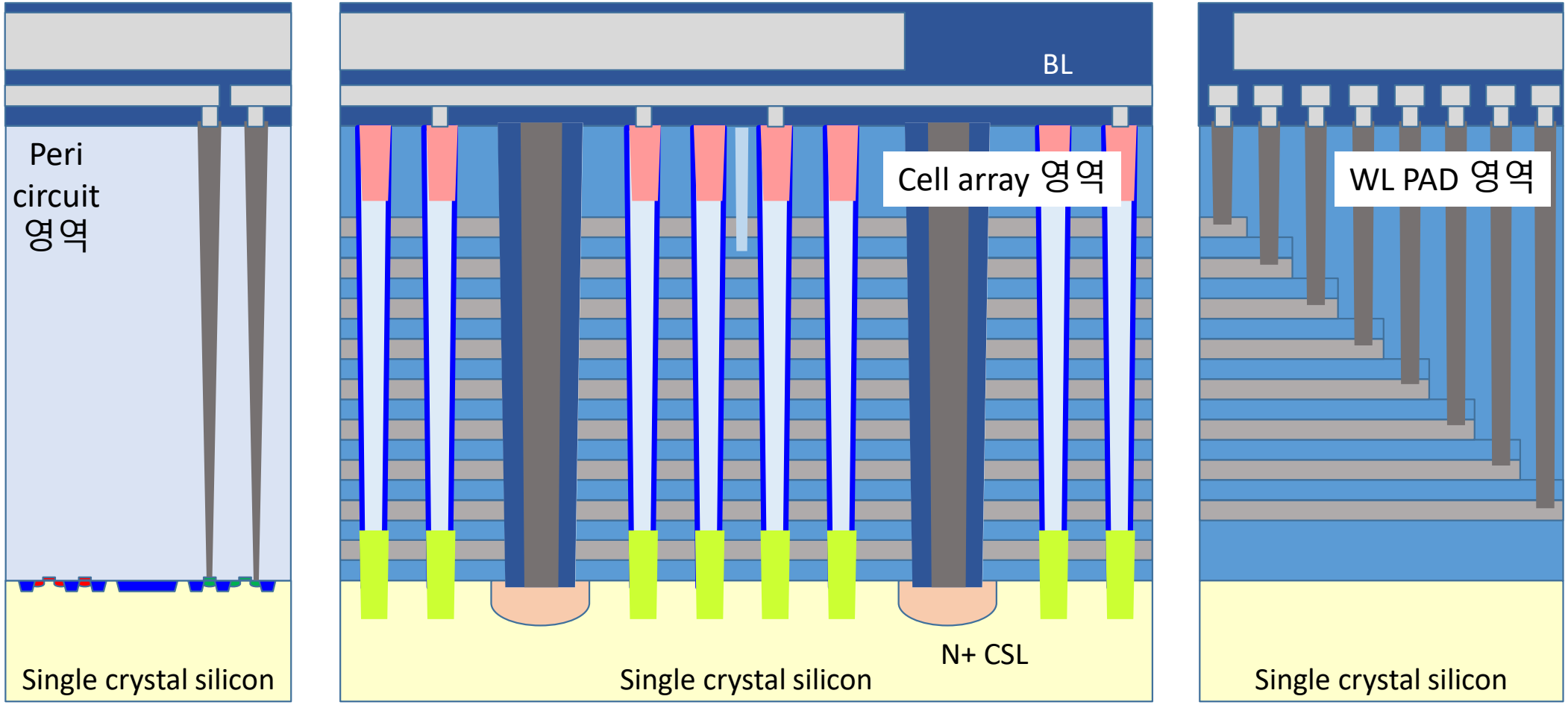


3D NAND Flash Memory – Process Integration

• 7. Contact 형성

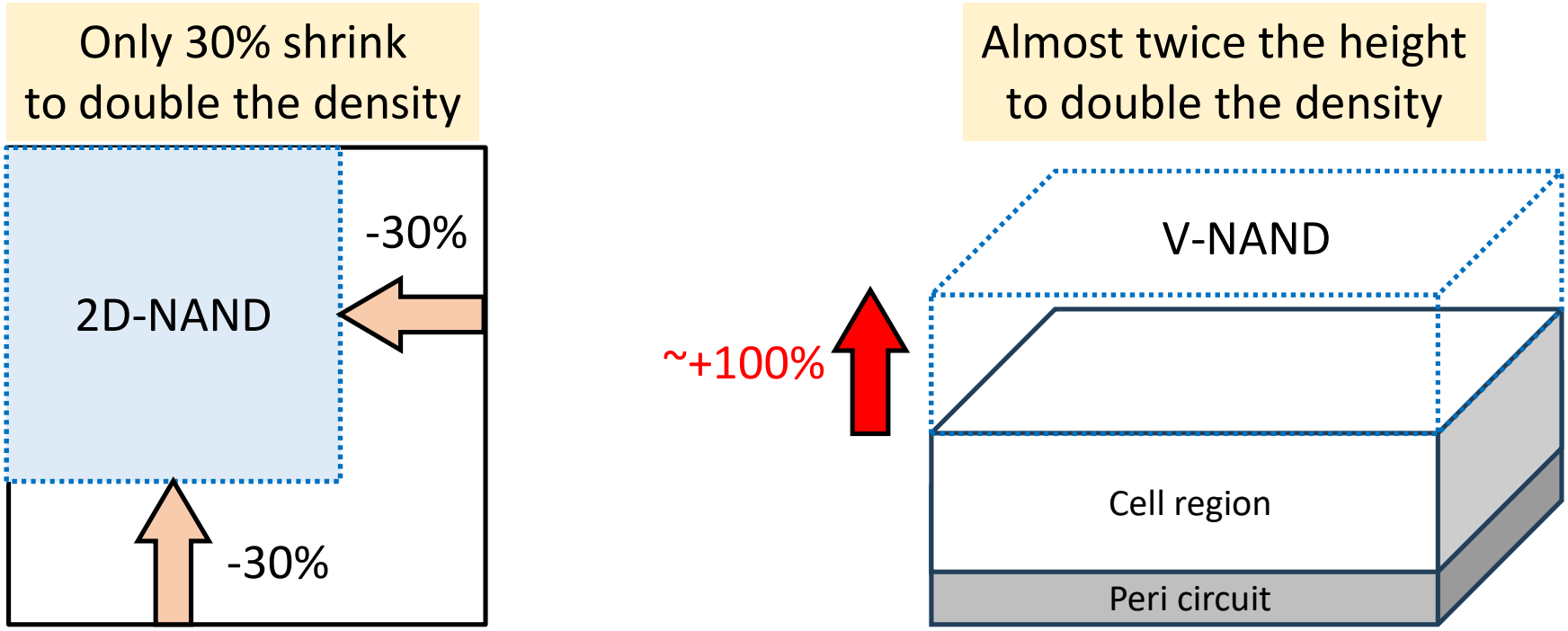


3D NAND Flash Memory – Process Integration(배선)



3D NAND Flash Memory – Density doubling

- Planar NAND 에서는 x/y 방향으로 공정 부담을 나눠가짐
- 3D NAND에서는 x/y 방향 대비 z 방향에 훨씬 더 큰 부담이 가해짐



3D NAND Flash Memory – Bit cost 개선 방법

- Layer 수를 지속적으로 증가시키기 위해 다양한 방법을 도출/적용 중

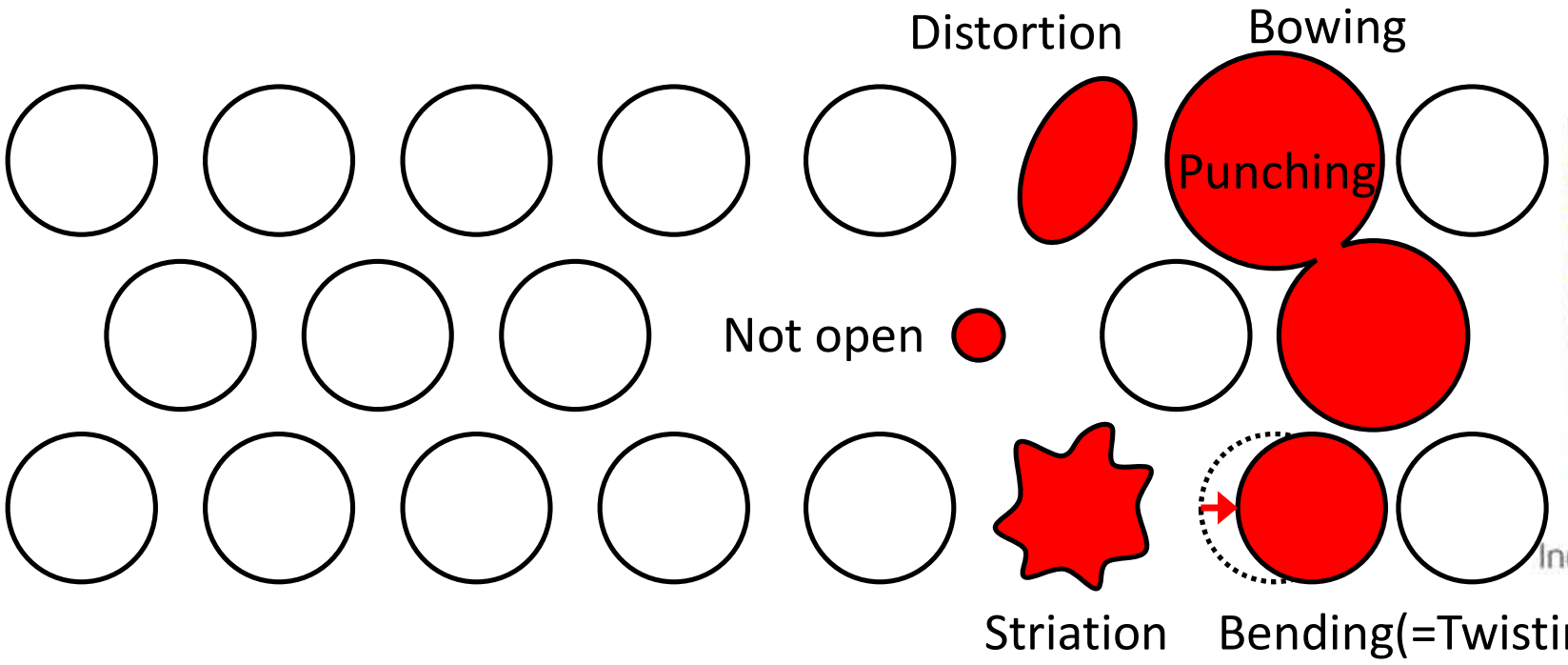
Category	세부항목	설명
Layer 수 증가	High aspect ratio etch 개선 (Channel hole, WL cut, 각종 contact들)	극저온 etch 등의 새로운 공정/설비 개발
	Mold scaling (Transistor scale down)	ON mold의 두께를 감소하여 etch burden 감소 Cell transistor의 특성/신뢰성이 허용하는 범위 내에서 지속적으로 scale down
	Multi-deck	Channel hole을 한 번에 etch하지 않고 두 번 이상에 나눠서 etch하여 etch 난이도 감소
Chip 면적 감소	CMOS Under Array CMOS Bonded Array	CMOS 회로를 cell array 아래로 넣어 면적 감소 CMOS 회로를 따로 제작하여 NAND wafer와 bonding
	Multi-hole	WL-cut 사이에 들어가는 hole 개수를 늘려 WL-cut이 차지하는 비율을 감소시켜 chip size 감소
	WL pad 면적 감소	X/Y trim & etch 및 hybrid trim & etch

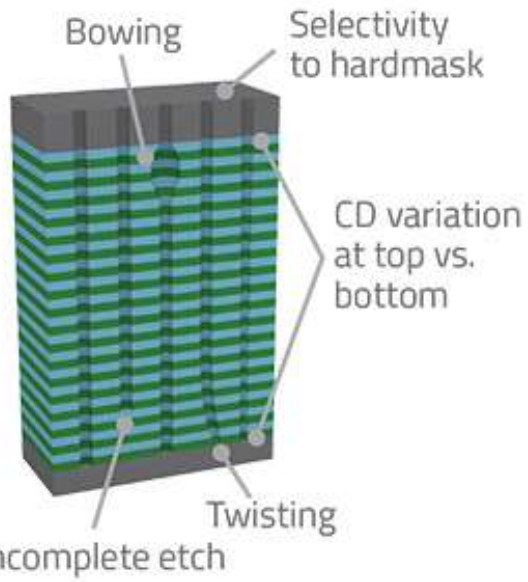
3D NAND Flash Memory – Channel hole

- 3D NAND의 대부분의 문제는 channel hole으로부터 기인함

Ideal channel hole profile

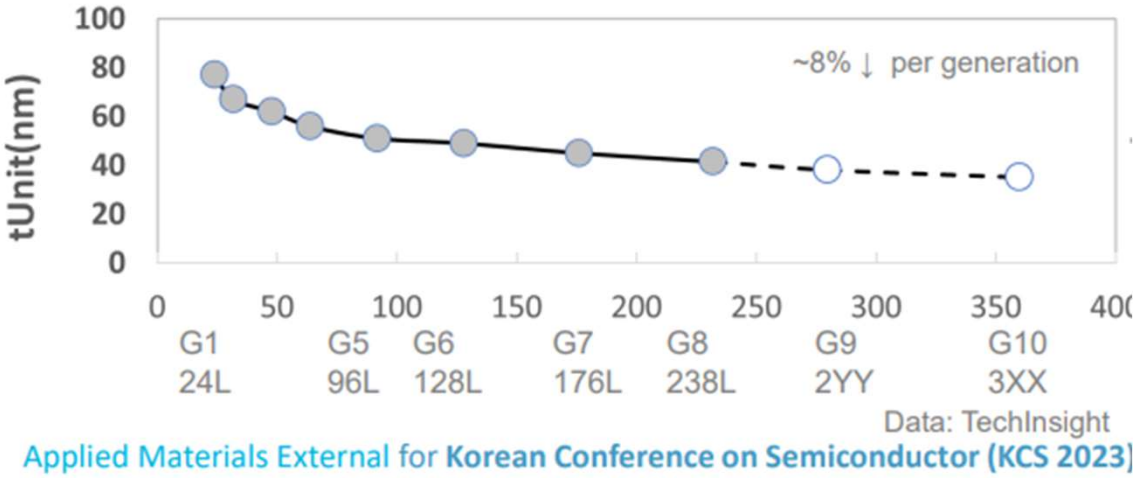
In reality



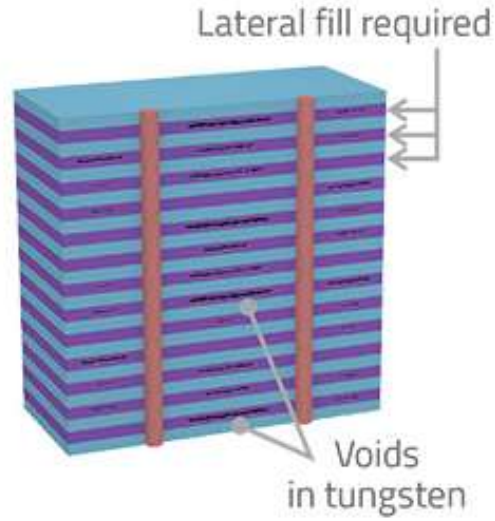


3D NAND Flash Memory – Mold scaling

- Layer 수 증가에 따른 전체 높이 증가를 완화하기 위해 지속적으로 mold scaling을 하고 있음.
- Cell transistor의 Lg/Ls 감소 다른 특성 열화로 인해 포화 상태
- WL W replacement 공정 상의 불량도 주요 고려 항목

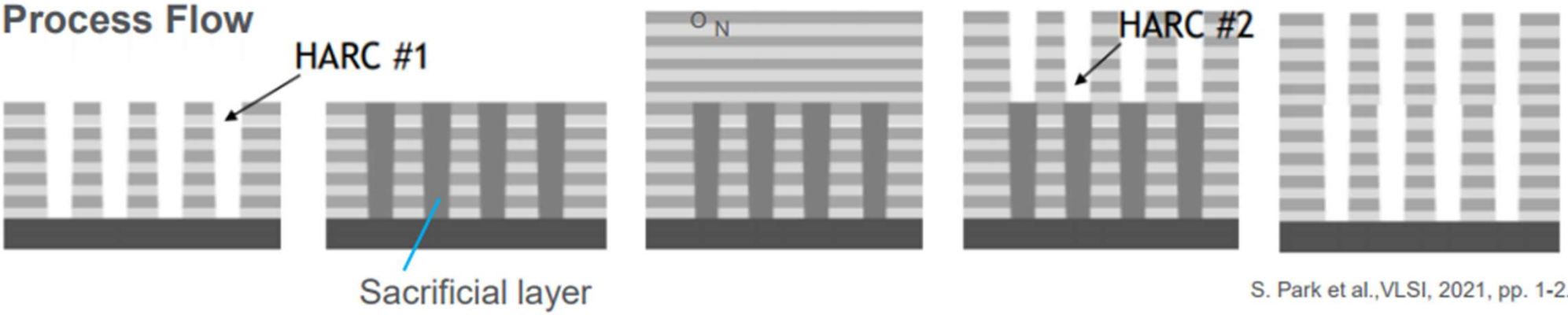


Applied Materials External for **Korean Conference on Semiconductor (KCS 2023)**



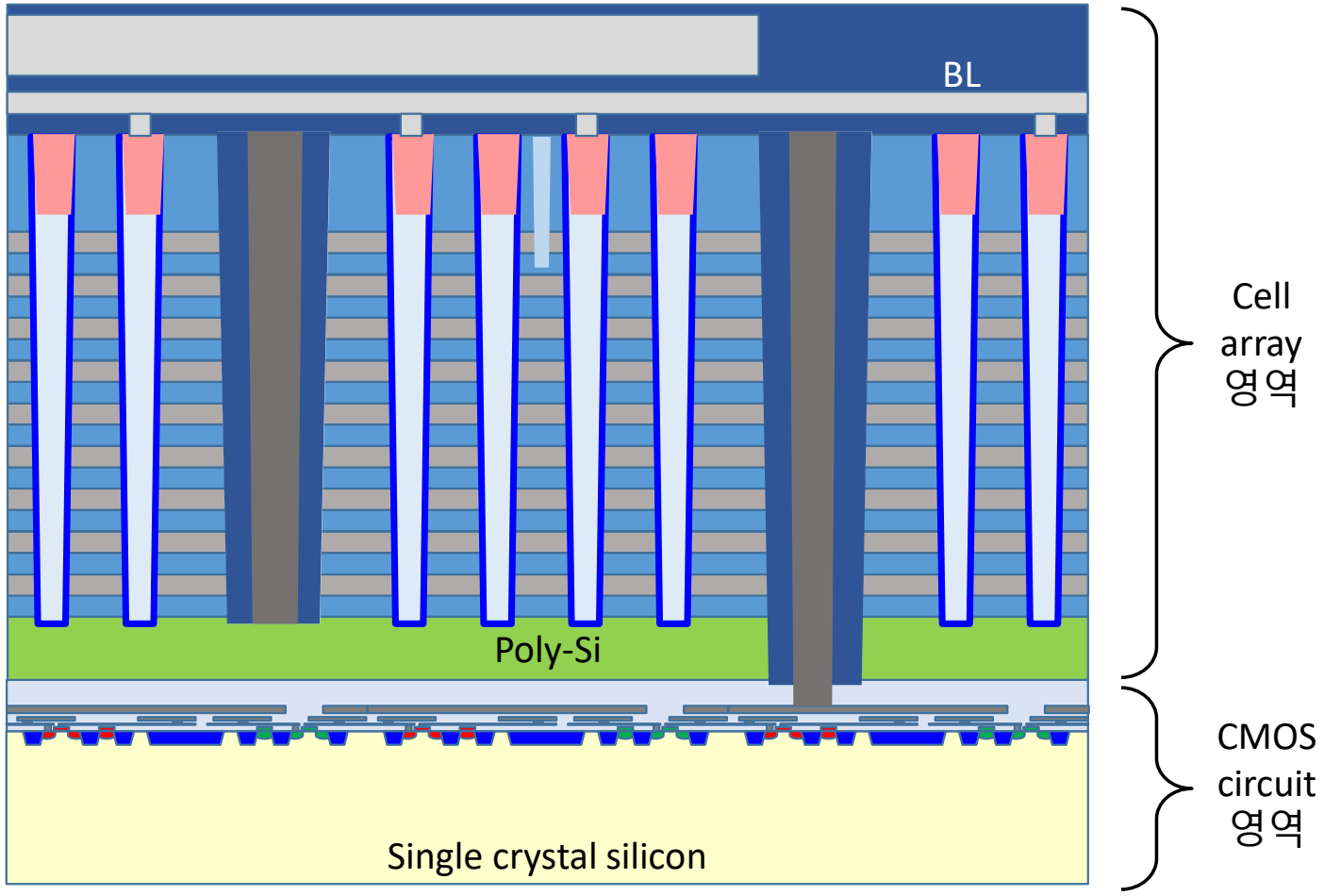
3D NAND Flash Memory – Multi-deck

- Channel hole을 한 번이 아닌 여러 번에 나눠서 etch하는 scheme
- Micron이 176L에서 2-deck scheme을 처음으로 적용
- 공정 비용 및 misalignment 문제 극복 필요

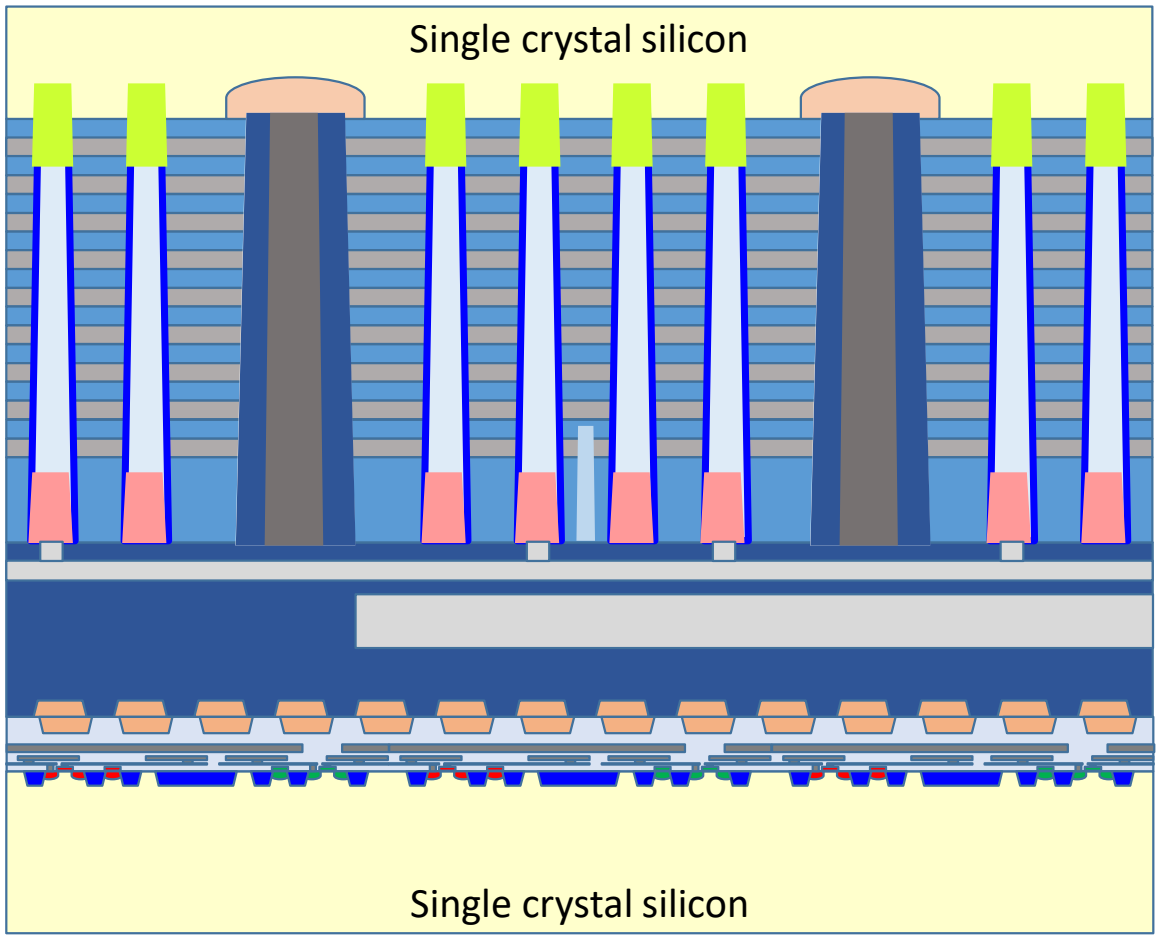


S. Park et al.,VLSI, 2021, pp. 1-2.

3D NAND Flash Memory – CMOS Under Array



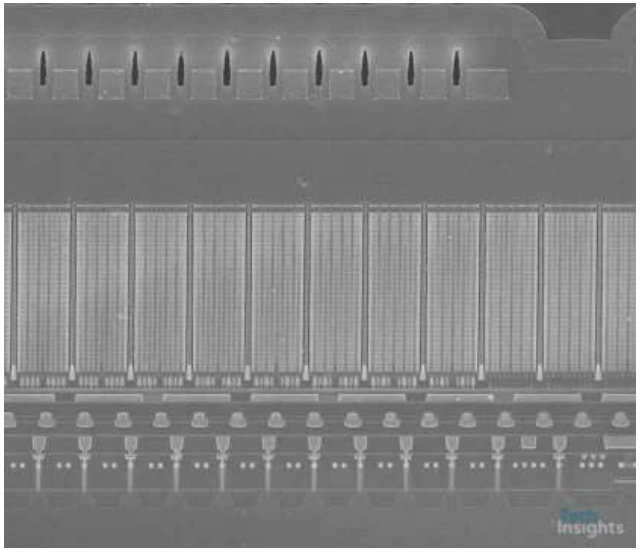
3D NAND Flash Memory – CMOS Bonded Array



Cell array wafer

Wafer bonding

CMOS circuit wafer

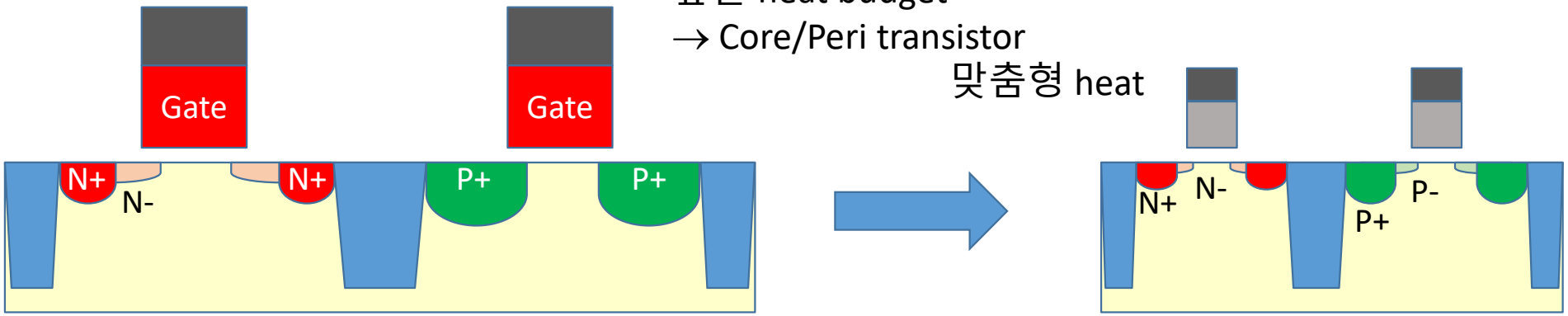


[YMTC's NAND with CBA]

3D NAND Flash Memory – CMOS Bonded Array

- Cell array 제작 공정에 들어가는 높은 heat으로 인해 peri transistor의 scaling에 한계가 있음.
- Chip size 감소 및 I/O speed 증가를 위해 peri/core transistor의 scaling 필수

Cell transistor 특성 개선 위한
높은 heat budget
→ Core/Peri transistor
맞춤형 heat

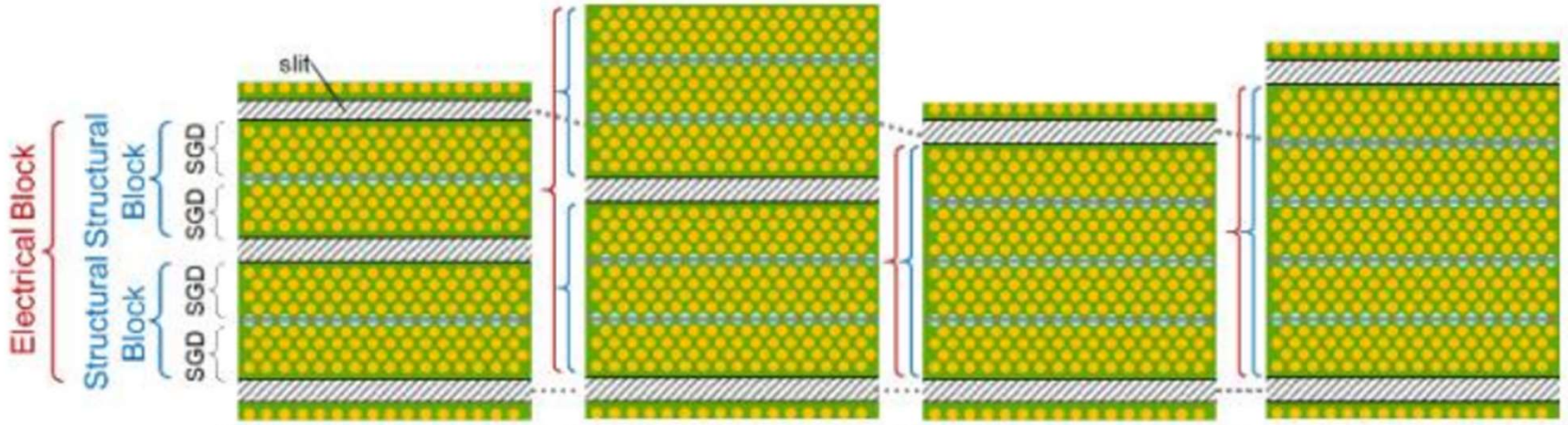


[현재의 LV transistors]

[CBA 적용 시 LV transistors]

3D NAND Flash Memory – Multi-hole

- Channel hole 사이에 있는 WL-cut 면적의 비율을 줄여서 chip size 개선

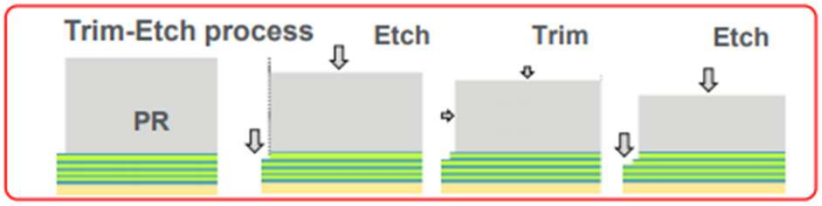


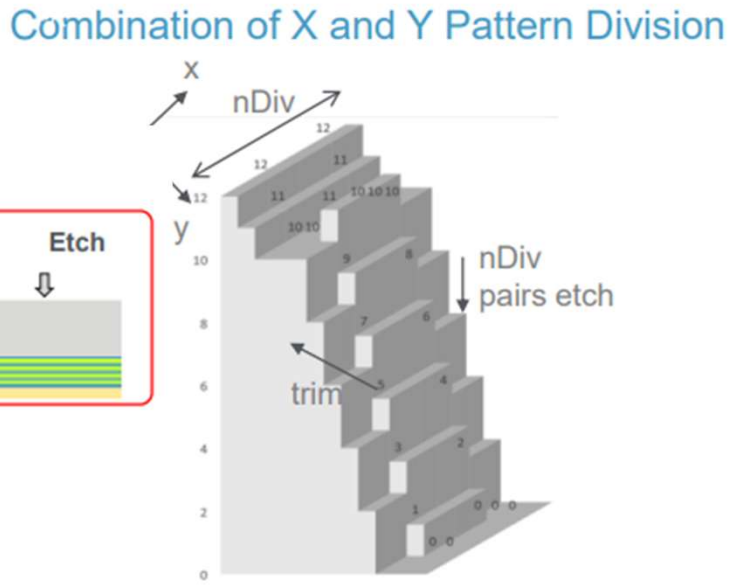
#Pillar / Structure	9-pillar	14-pillar	19-pillar	24-pillar
#SGD / Structure	2 SGD	3 SGD	4 SGD	5 SGD
#SGD / Block(elec)	**4 SGD** (to 8 SGD)	6 SGD	**4 SGD** (or 8 SGD)	5 SGD
XY area scaling	100%	94%	91%	89%

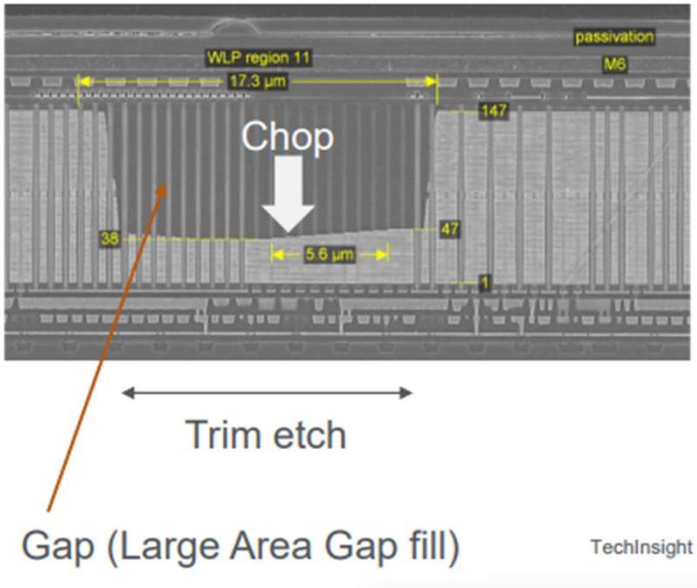
Russ Meyer et al., iedm 2022, pp 599-602

3D NAND Flash Memory – WL-pad 면적 감소

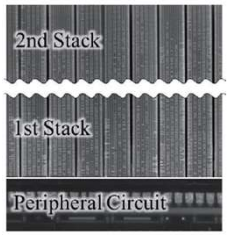
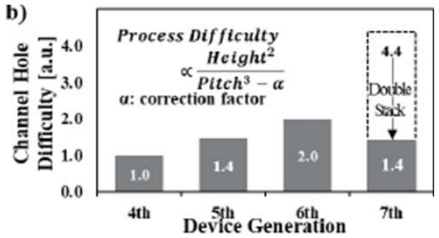
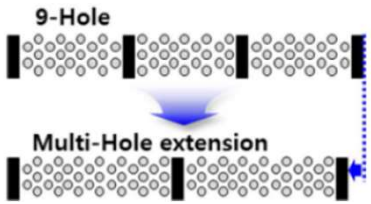
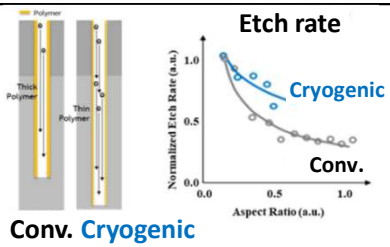
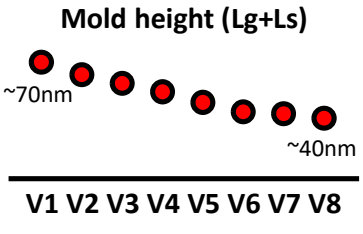
- WL별 pad를 형성하는데 필요한 lithography 횟수 및 면적 감소 필수
- 한방향 trim&etch → X/Y 방향 trim&etch



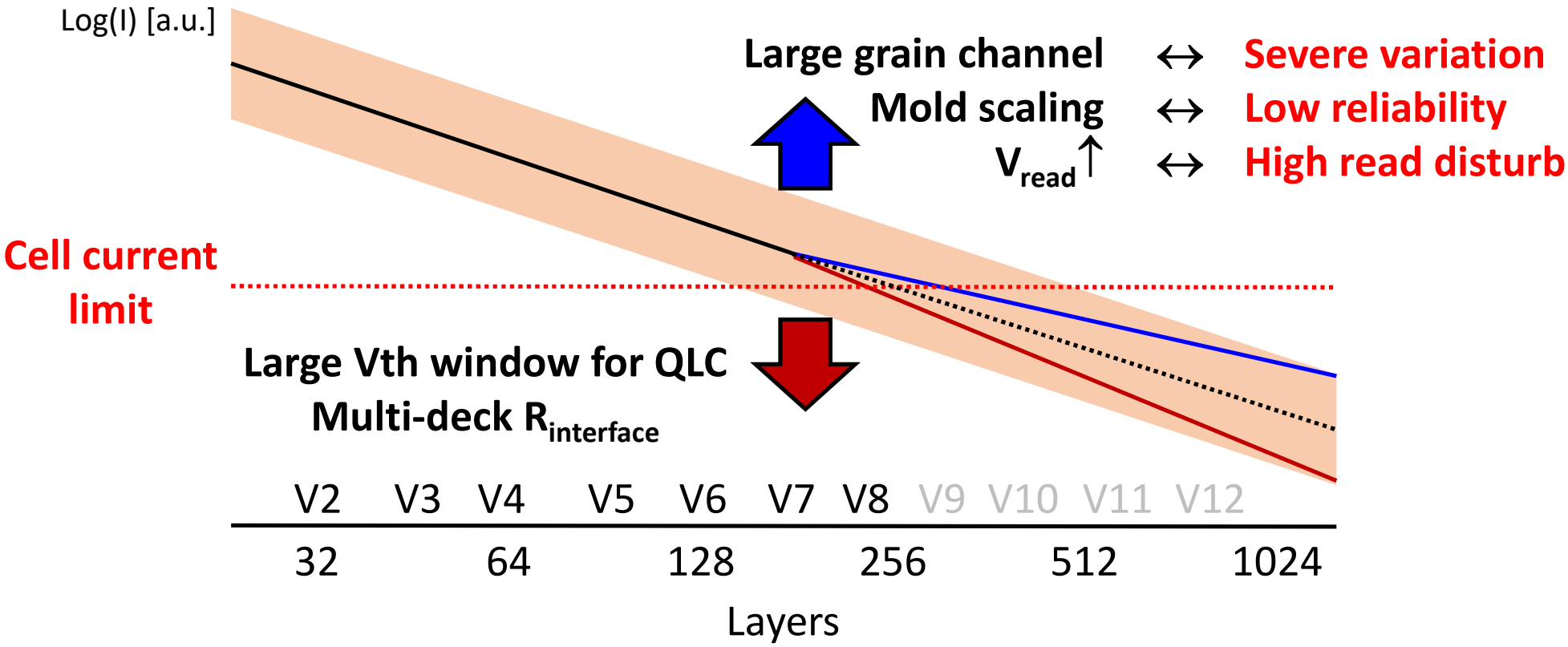




3D NAND Flash Memory – Summary of Issues

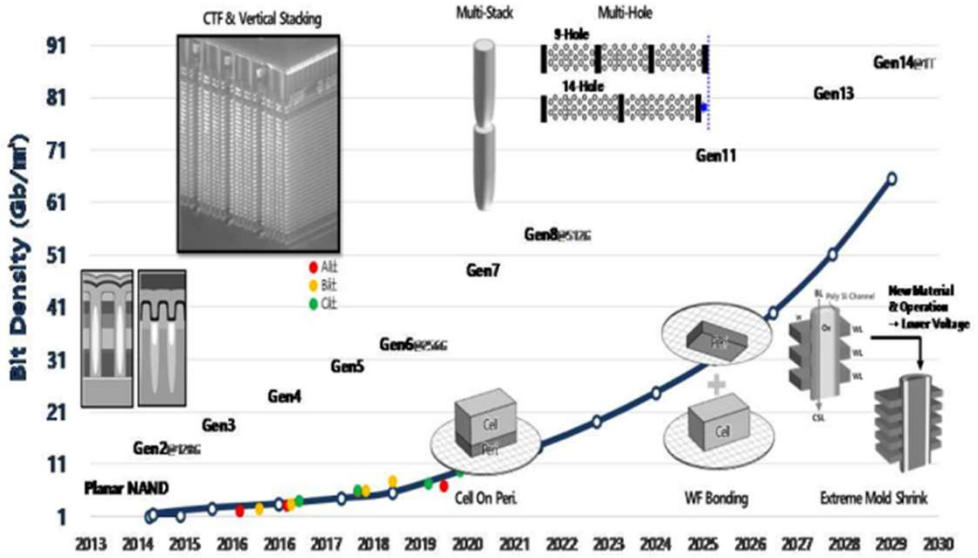
Architecture			Process	Device
CUA (CMOS under array)	Multi-deck	Multi-hole	Cryogenic etch	Lg/Ls scaling
Lateral scaling # of layers↓	Etch depth↓	Lateral scaling # of layers↓	Etch rate↑	Etch depth ↓
 				
One-time only	High cost High channel R at the interface	Small gain Worse WL W fill Large block size	Uniformity	Worse interference &reliability

3D NAND Flash Memory – Device Issues



3D NAND Flash Memory – Future Prospect

- Multi-deck/multi-hole 증가
- CMOS-Bonded Array
- Channel의 새로운 crystallization
- 새로운 물질/구조를 이용한 Cell transistor 특성/신뢰성 개선
- 그럼에도 불구하고 너무나도 빨리 증가하는 공정 난이도…



[K. Kim, IEDM 2021]

- 3D NAND 이후의 새로운 메모리 시스템은?

감사합니다.

References:
1. Inside Solid State Drives (SSDs) edited by Rino Micheloni, Alessia Marelli, and Kam Eshghi, Springer, 2013
2. 3D Flash Memories edited by Rino Micheloni, Springer, 2016