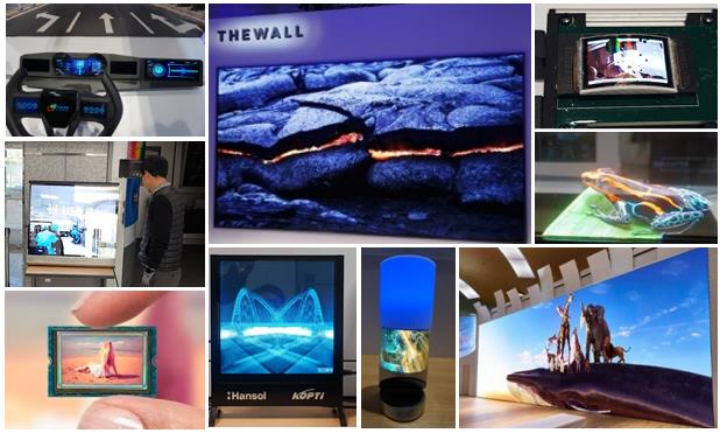
마이크로LED 기술 동향



2024. 06

Photonic Semicondutor & Display Research Division
(MicroLED Display, Nano-LED, Laser Diode, Sensor, GaN Semiconductor)

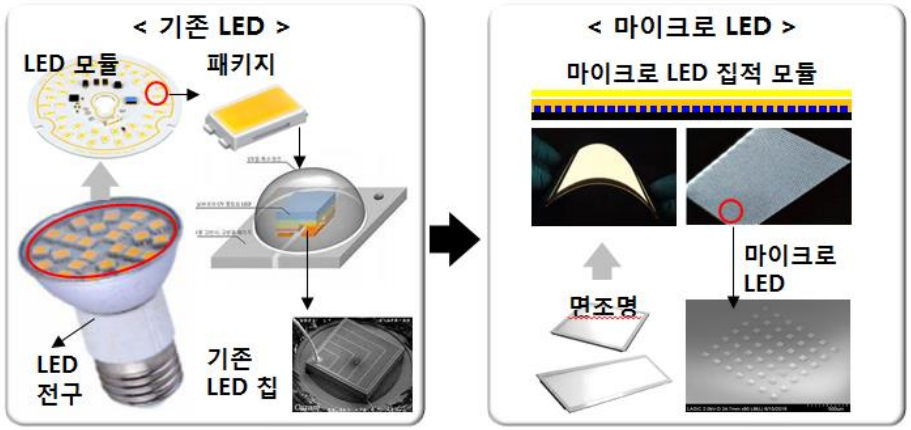
Korea Photonics Technology Institute

Research Director
Y.W. Kim, Ph.D.

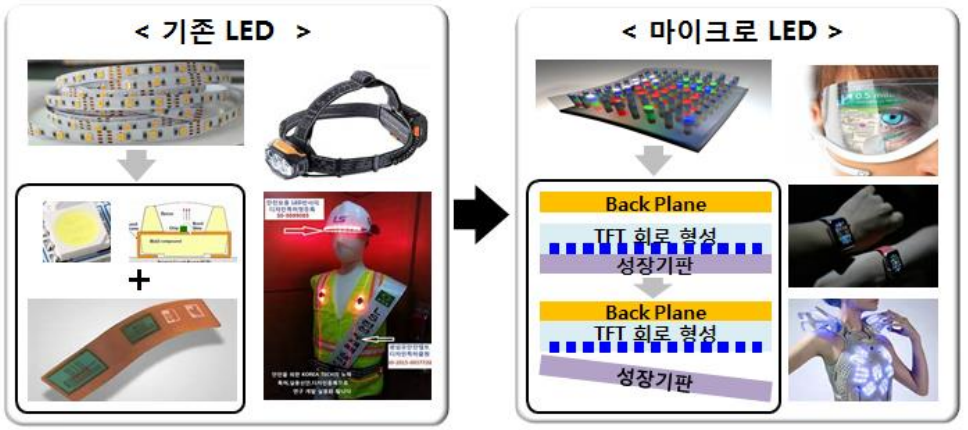
01 Overview

Micro LED Application

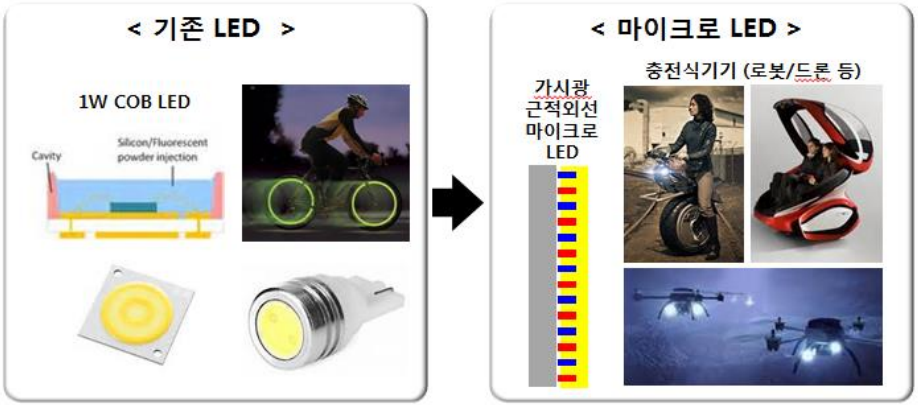
[Lightings]



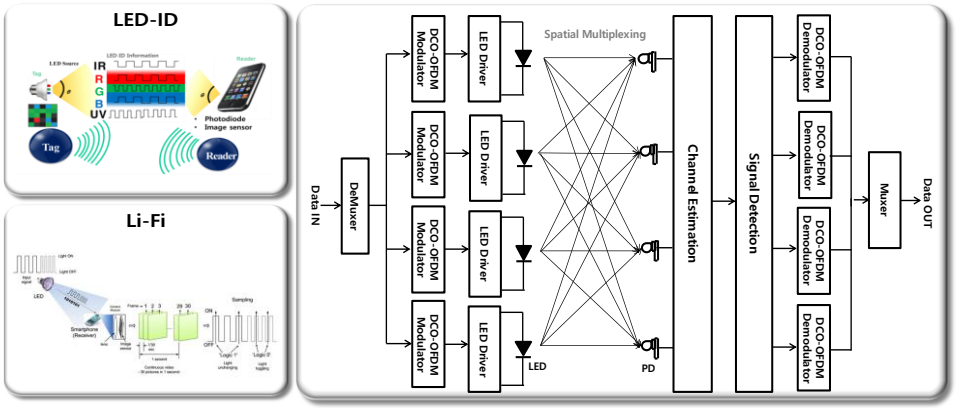
[Wearable]



[Drone/Robot]



[Telecom.]

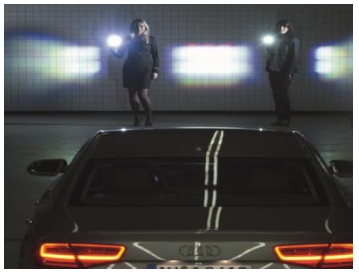


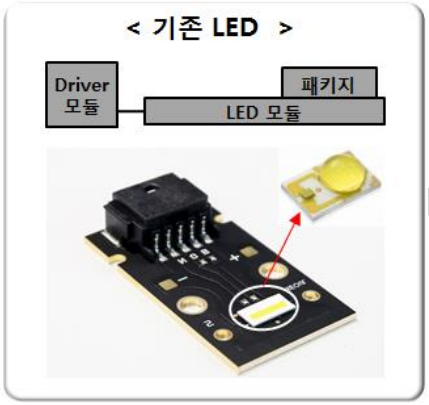
* Reference : n-tech Research Report, Micro-LED Market Opportunities: 2018-2027

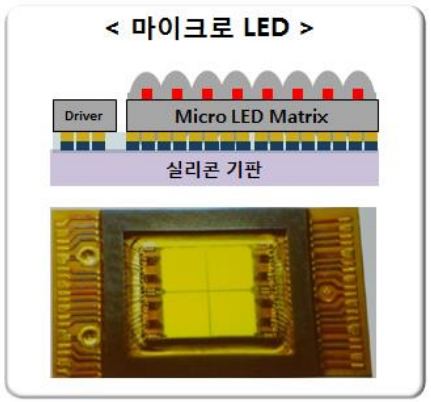
01 Overview

Micro LED Application

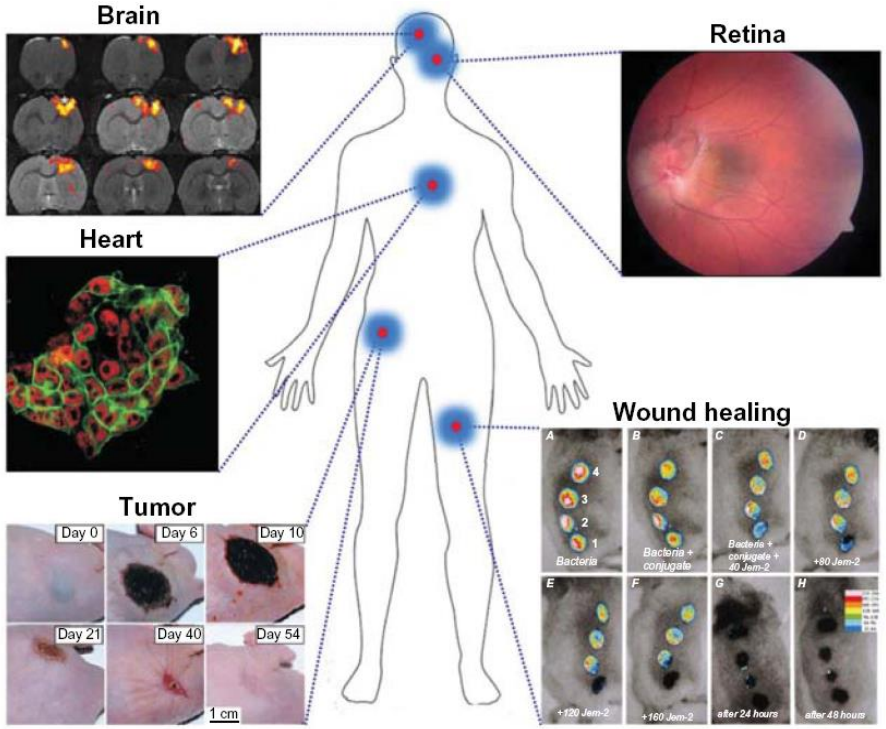
[Automotive – Headlamp, Lidar, Sensor]

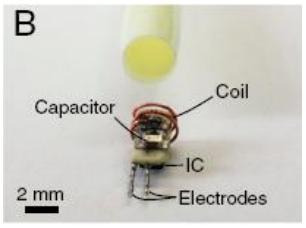


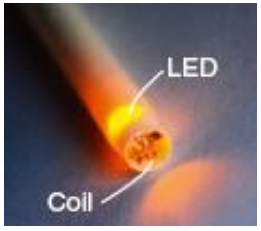




[Bio. / Medical]





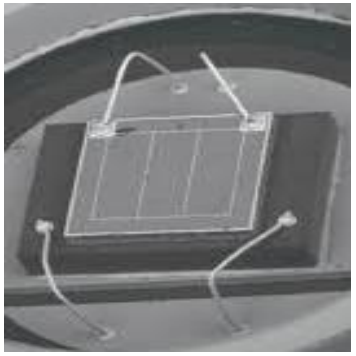


01 Overview

Chip Size Vs. Application

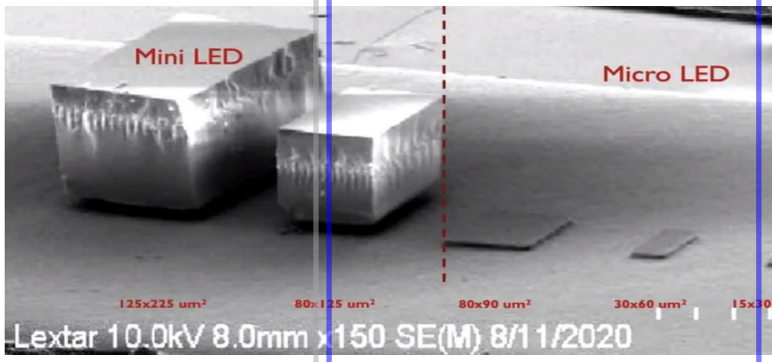
~ `18 ~ `30

[LED (< 1mm)]

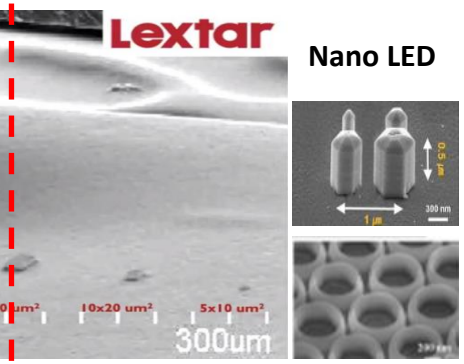


[Mini-LED (< 200 um)]

[MicroLED(< 100 um)]



[Micro+Nano LED(< 10 um)]

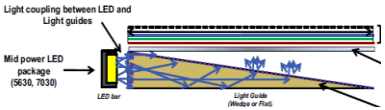


Conventional Tech.

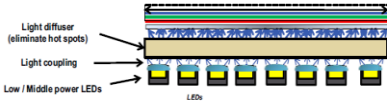
New Tech.

Challenging Tech.

[Edge Emitting Type]



[Direct Emitting Type]



[Video Wall, Digital Signage, 전광판]

New Paradigm

[TVs]

[Smart Watch]

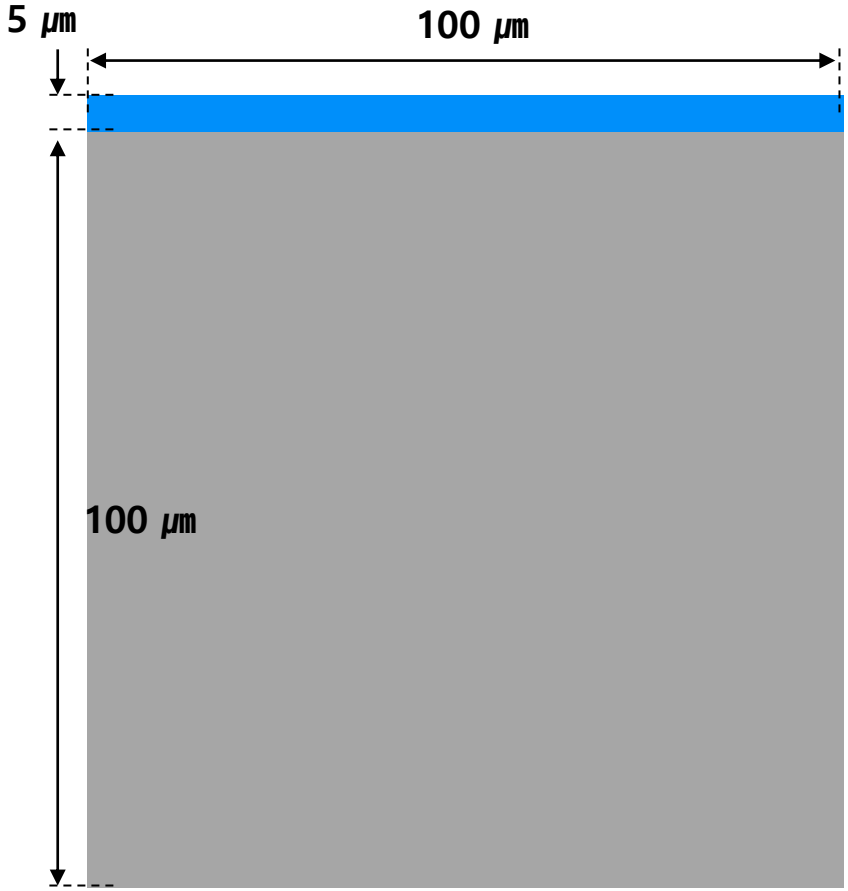
[Navigation]

[Smart Glass]

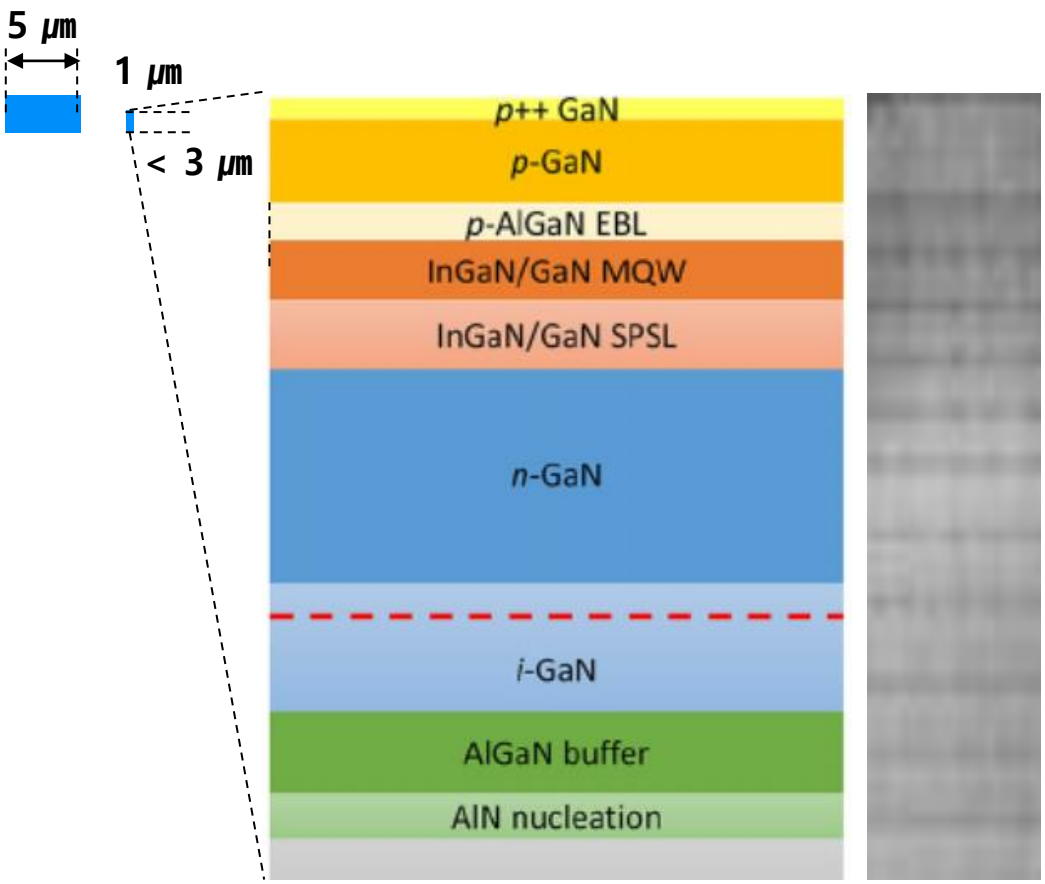
01 Overview

LED Vs. MicroLED

[Mini-LED]



[Micro-LED]

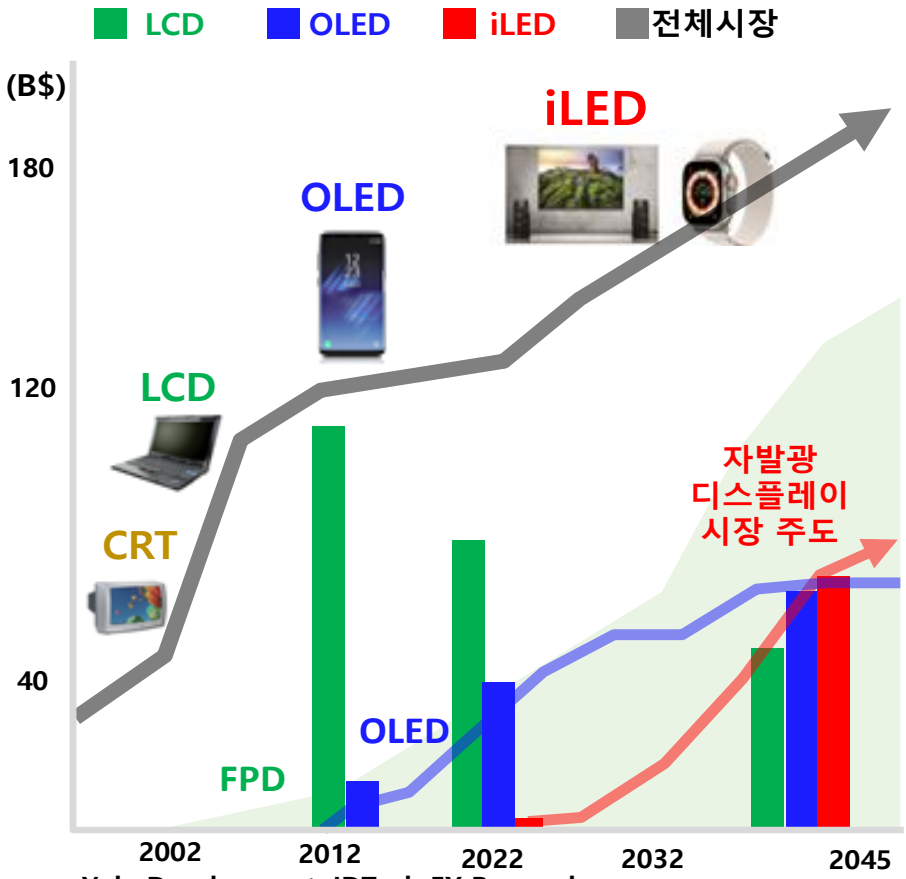


* EBL : Electron Blocking Layer SPSL : Short-Period SuperLattice

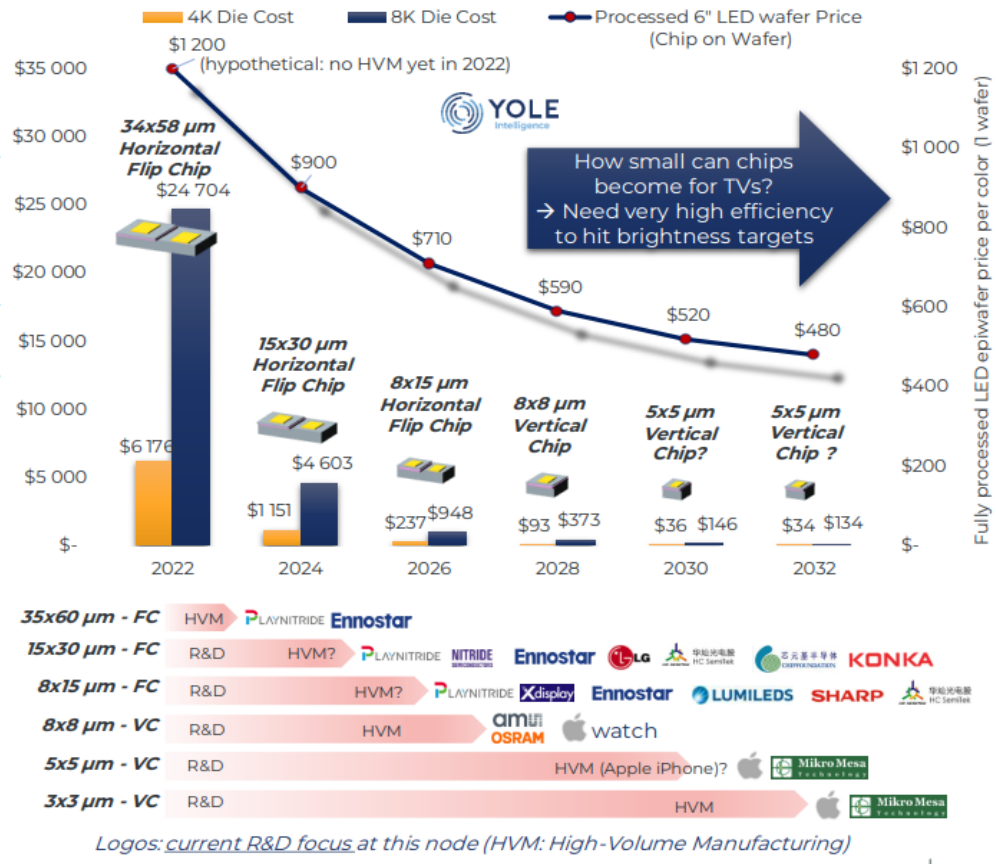
01 Overview

Market Trend & Cost Road Map

구분	2023	2027	2032	2037	2045
LCD	768.5	812.5	734.7	611.6	454
OLED	467.3	577	498.8	624.1	659.4
Micro LED	0.3	19.6	160.1	415.7	799.8
Others	5.6	5.8	29.4	52.4	63
합계	1,241.7	1,414.8	1,423.0	1,703.7	1,976.3



		화소	패널	모듈	기타	합계
`22		15,977	8,993	381	1,257	26,608
`28		389	1,872	226	480	2,967
`32	최소	165	417	158	238	978
	최대	366.8	1726.2	219.5	455.4	2768

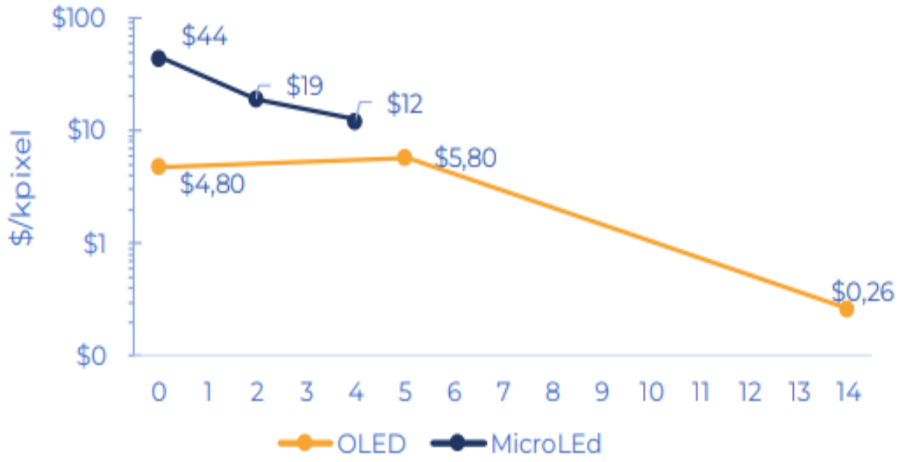


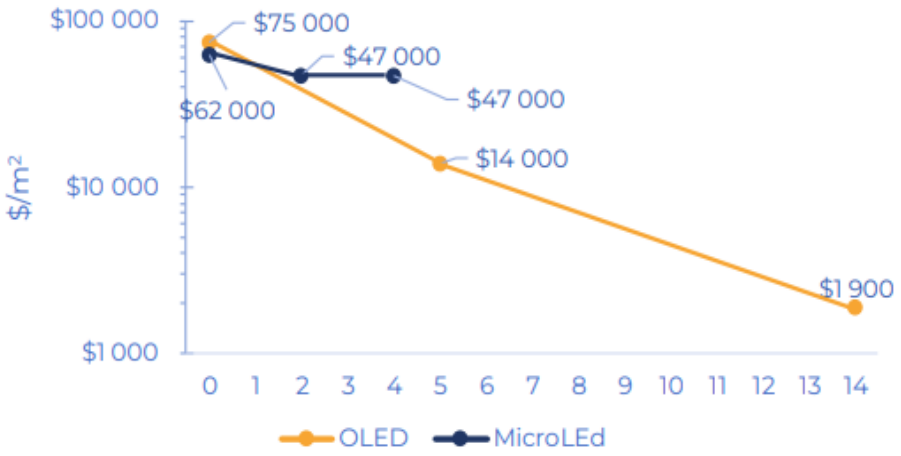
* Source : Yole Development, IDTech EX Research

01 Overview

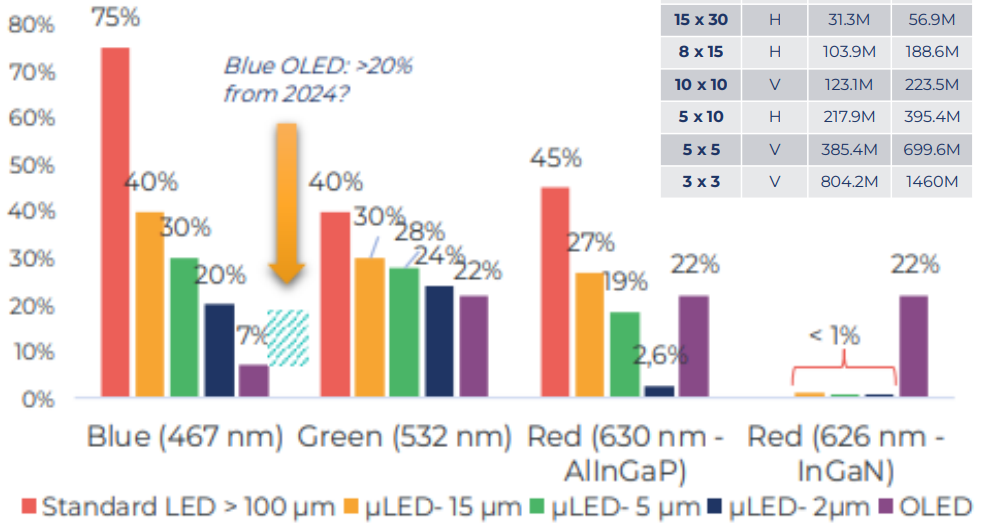
Cost : OLED Vs. MicroLED → Efficiency & Quality

Determination of adaptable Cost





Die size	Die type	150 mm	200 mm
34 x 58	H	7.7M	14M
20 x 40	H	18.2M	33.1M
15 x 30	H	31.3M	56.9M
8 x 15	H	103.9M	188.6M
10 x 10	V	123.1M	223.5M
5 x 10	H	217.9M	395.4M
5 x 5	V	385.4M	699.6M
3 x 3	V	804.2M	1460M



Number of pixels and dies per display (millions)

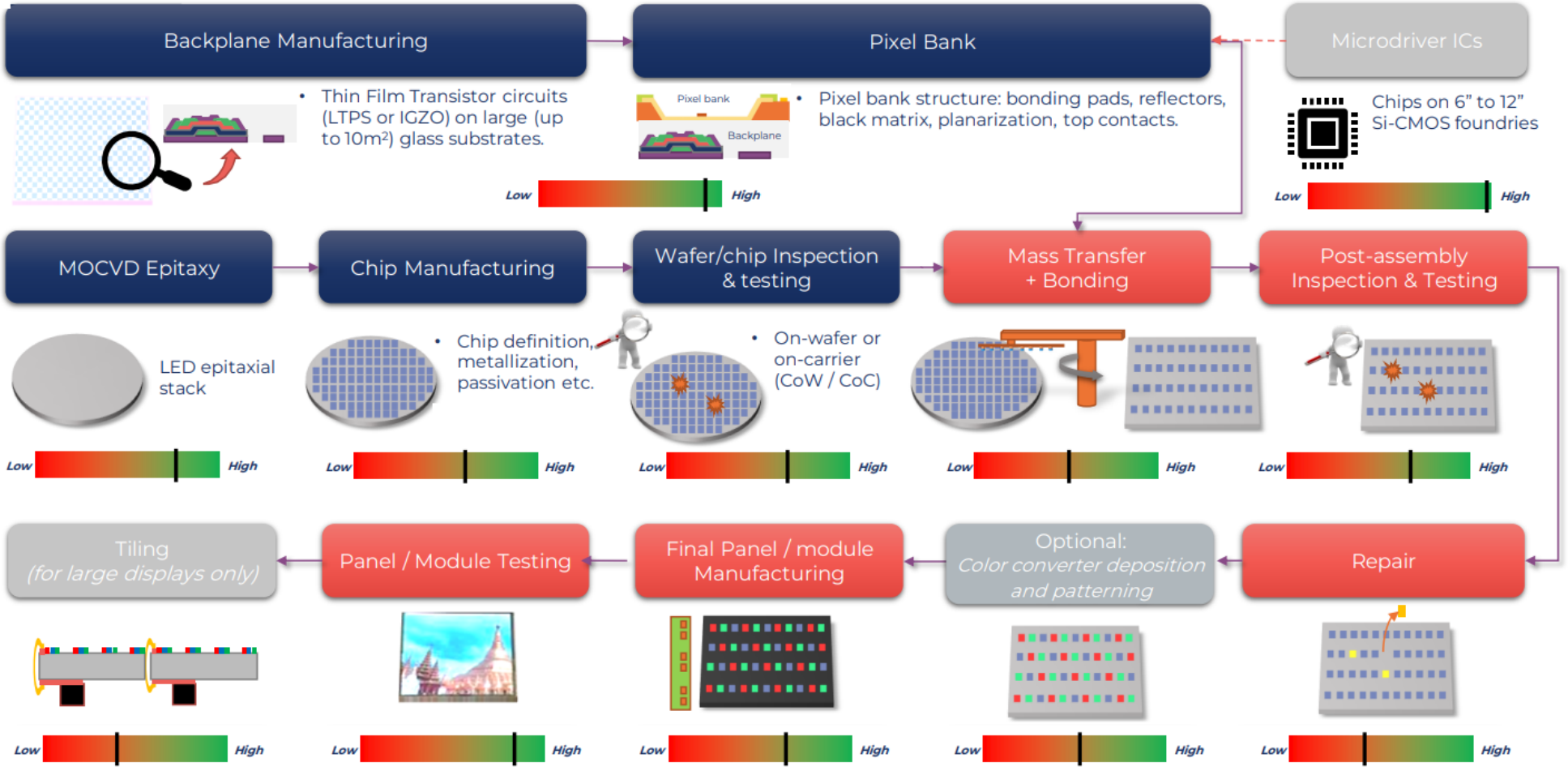
	4K	8K	iPhone 13 6.1”	iPad Pro 12.9”	Watch
Number of pixels	8.3M	33.17M	2.96M	5.6M	191.6k
Number of dies	24.9M	99.5M	8.9M	16.78M	575k

* Source : Yole 2022

02 MicroLED Display

Manufacturing Process : Maturity

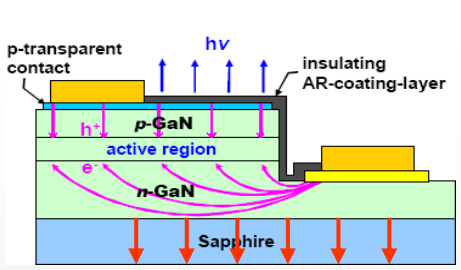
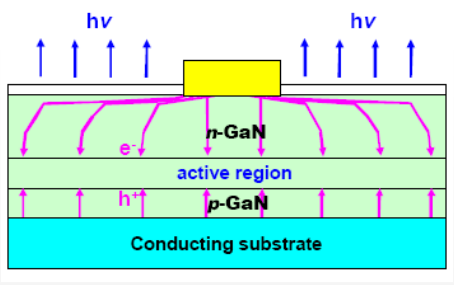
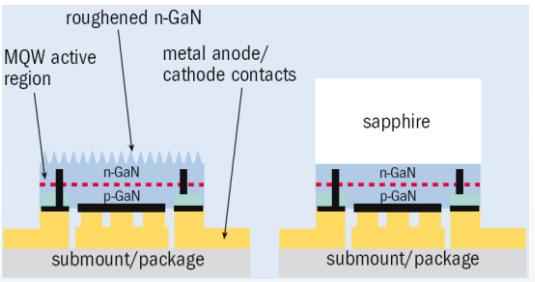
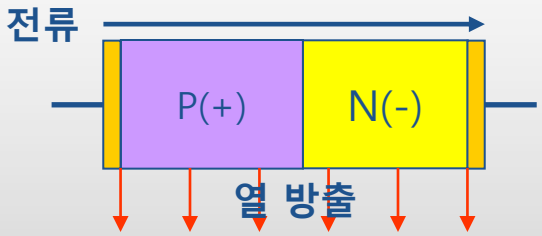
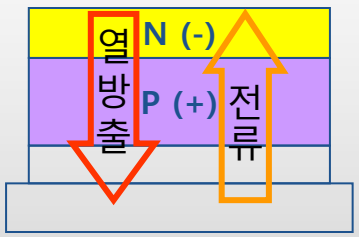
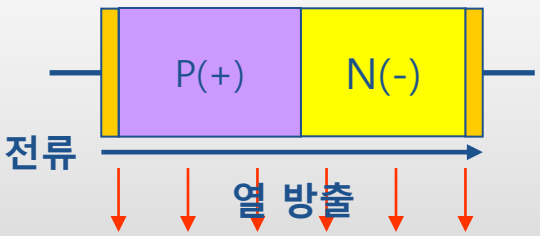
Needs new a technical solution below the middle level of maturity profile



* Source : Yole 2022

03 MicroLED Chip Production

Micro LED 정의 및 특징

	Horizontal Type	Vertical Type	Flip-Chip
구조			
전류 / 열방출			
장 점	전류와 열 방출 방향 분리 LED와 Metal 직접 접합 Heatsink까지 작은 열 저항	Receptor Wafer의 높은 열 전도도 (300 W/m-K 이상) 고효율의 광 추출 LED의 작은 열 저항	전류와 열 방출 방향 분리 Submount와 Metal 직접 접합 Heatsink까지 작은 열 저항
단 점	Carrier Wafer (Al_2O_3)의 낮은 열 전도도 : 20 ~ 35 W/m-K 전류 확산 → 낮은 광 추출 유기 접합제	전류와 열 방출 방향 동일 Electro- &Thermo- Migration Heatsink까지 높은 열 저항	Active – Submount 하단 까지의 열 전달 거리 증가 전류 확산 → 낮은 광 추출 Electro- &Thermo- Migration

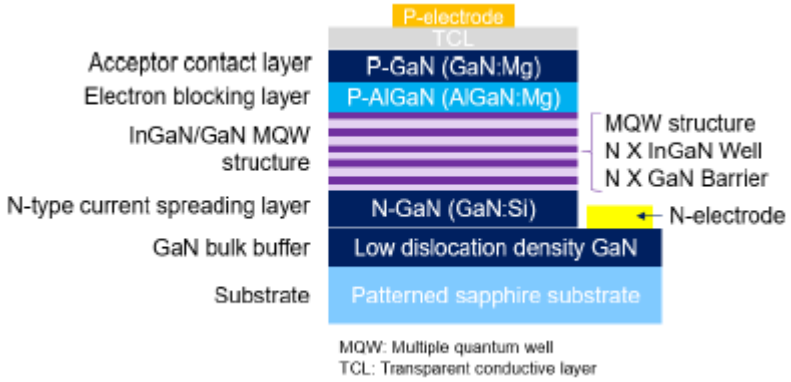
* Source : Yole 2022

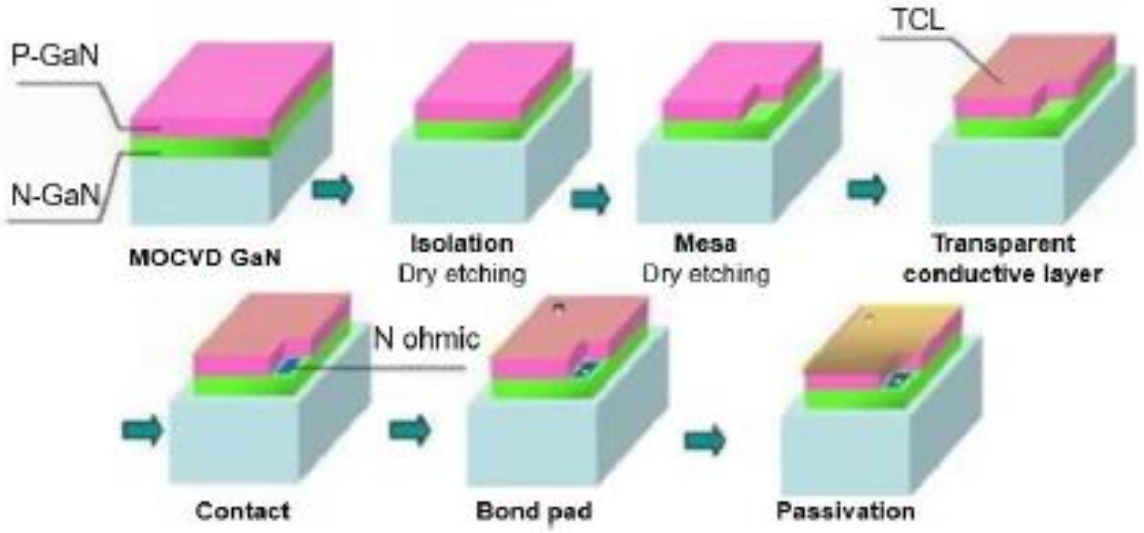
03 MicroLED Chip Production

Micro LED 칩 제조 공정

Lateral Type

- Then epitaxial layers are formed from undoped low dislocation density GaN, n-GaN, active multiple quantum well layers (MQW), p-AlGaN to p-GaN.
- Taking a later LED structure as an example, then the epi-wafer goes through photolithography and etching to form mesas. Then after ITO deposition, contact formation, substrate thinning, reflection layer deposition, the final LED arrays are formed.



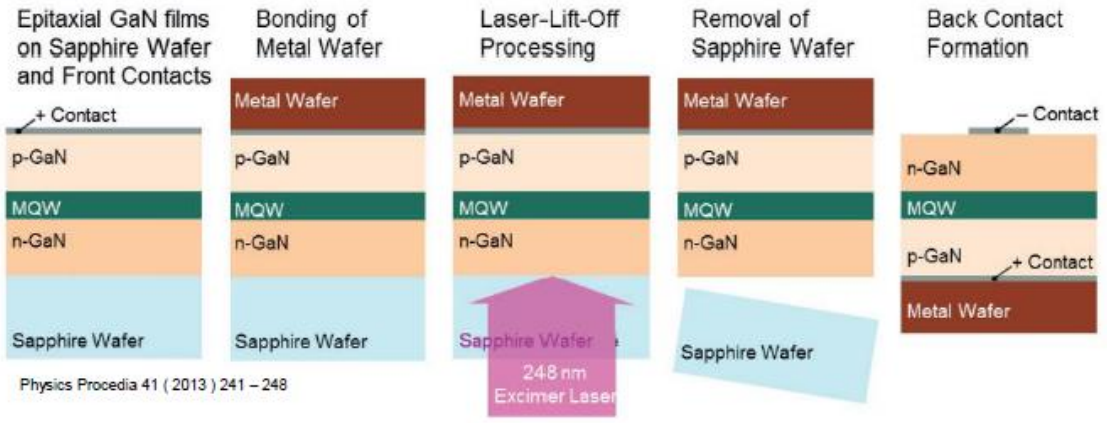


03 MicroLED Chip Production

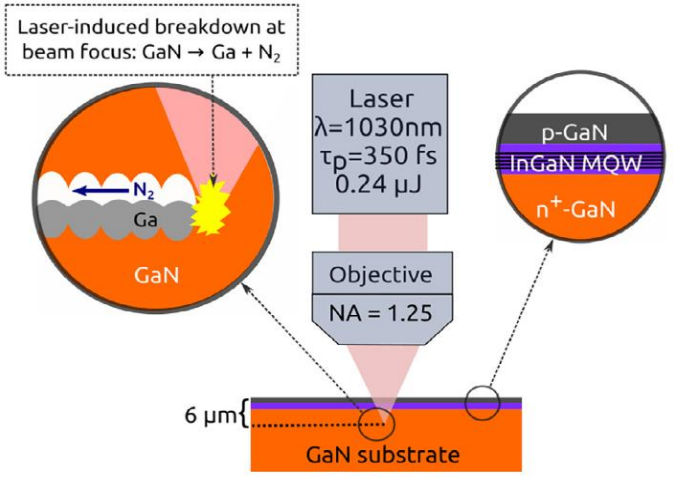
Micro LED 칩 제조 공정

Vertical Type

- After epitaxy, GaN epi-films are grown on sapphire wafer. P-contact is also deposited on top. Another substrate (e.g. metal) with better electrical and thermal conductivity is bonded to the p-contact. Then KrF excimer laser beams scan across the device. As sapphire is transparent to the wavelength of the excimer laser (248 nm), laser beams are absorbed by the interface between GaN and sapphire
- Sapphire substrate is then removed from the epi-film. Finally, the device is flipped for the n-contact (back contact) to be deposited on top.



Laser lift-off (LLO)

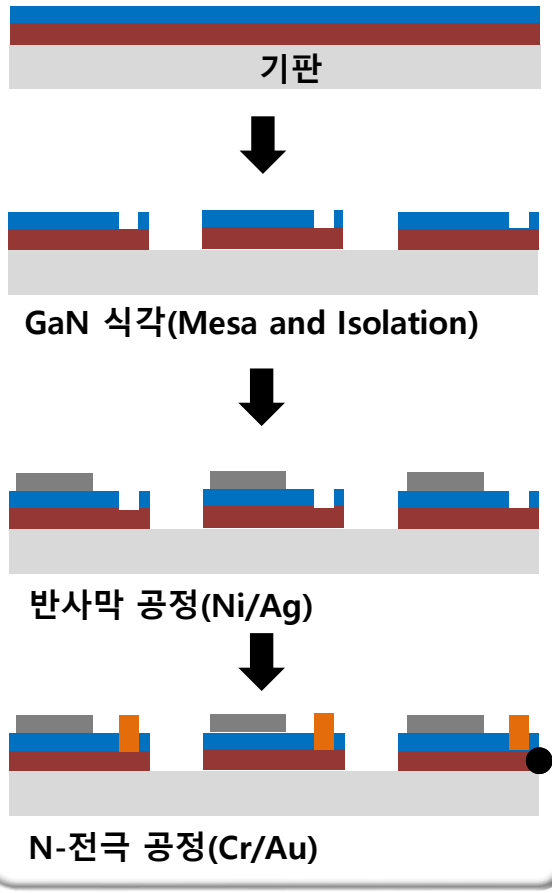


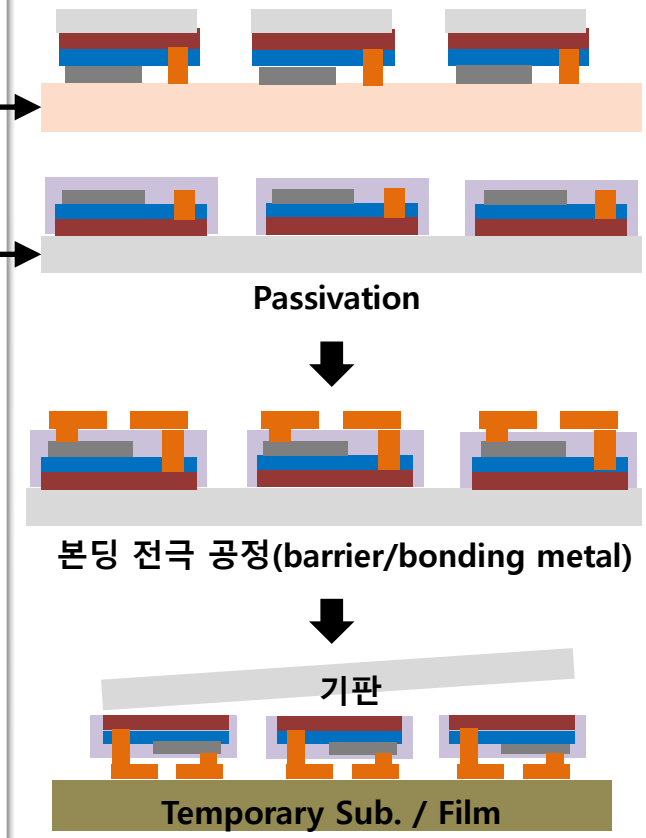
03 MicroLED Chip Production

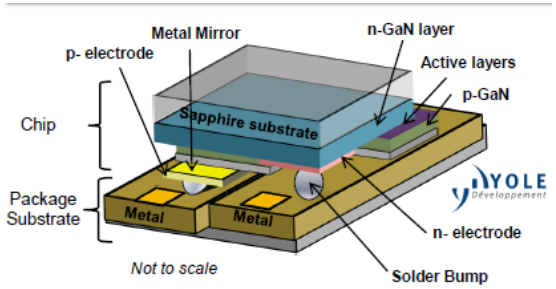
Micro LED 칩 제조 공정

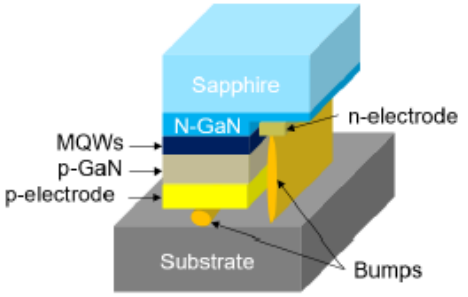
Flip-Chip Type

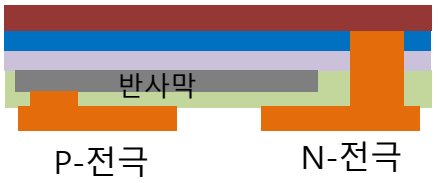
< 기존 공정 >







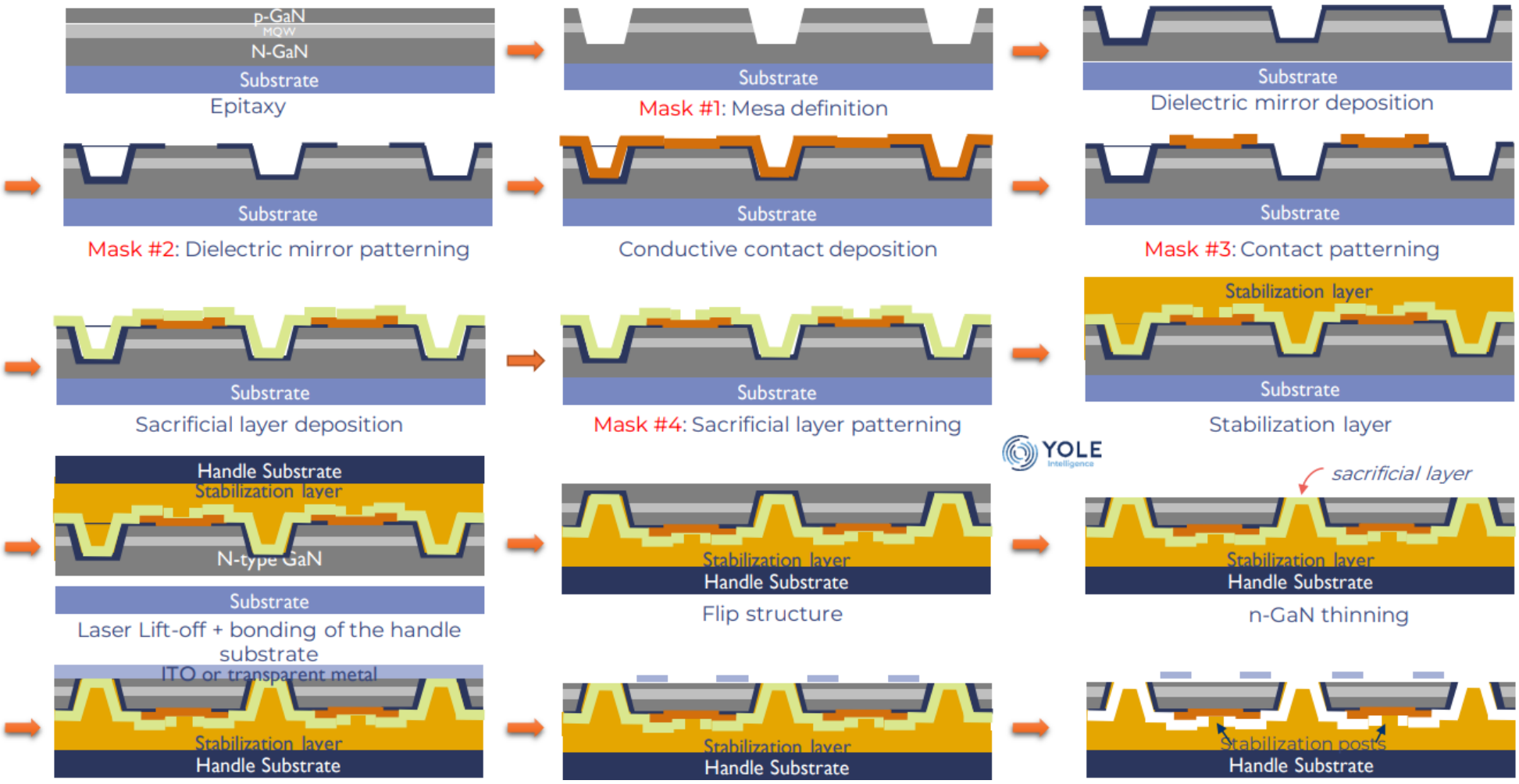




03 MicroLED Chip Production

Micro LED 칩 제조 공정

Flip-Chip including anchor for transfer & bonding



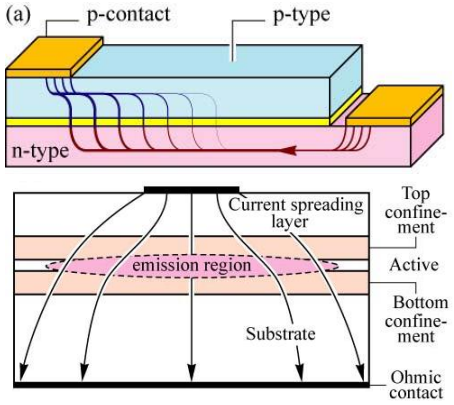
YOLE Intelligence

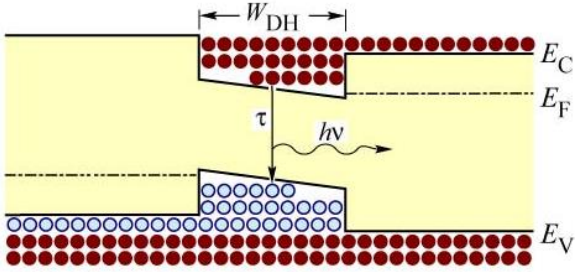
04 Epi. / Chip Fabrication

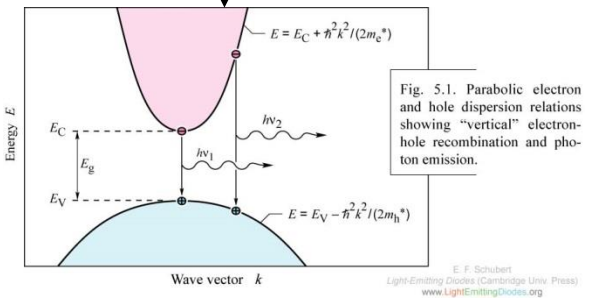
발광특성

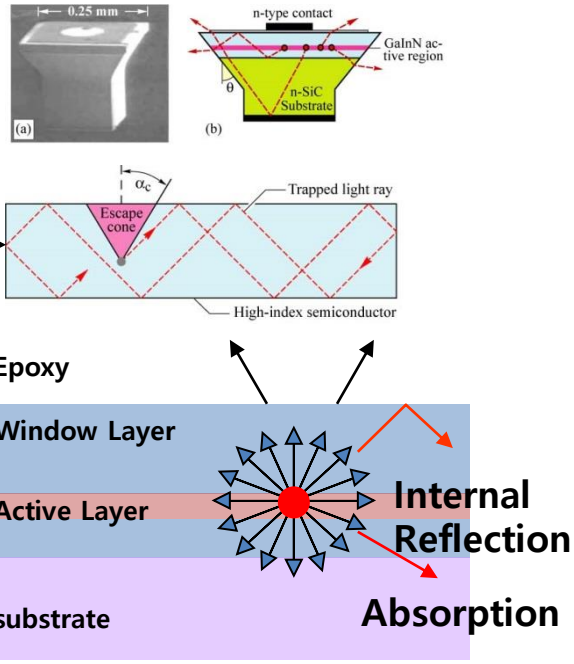
External Quantum Efficiency = $h_{injection} \cdot h_{internal} \cdot h_{extraction} \cdot h_{PKG}$

Epitaxtial Chip









04 Epi. / Chip Fabrication

Efficiency

Mechanism of Light Emission

- **External Efficiency**

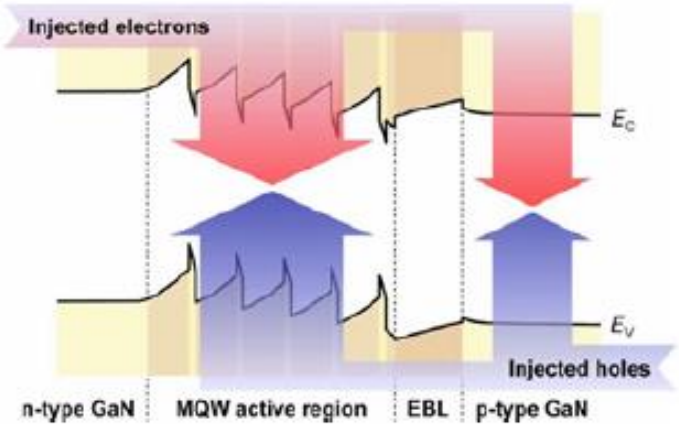
$$\eta_{ex} = \frac{\eta_{int} \times \eta_{extr} \times E_{photon}}{V_f \times q}$$

η_{ex} : 외부양자효율 E_{photon} : Photon에너지

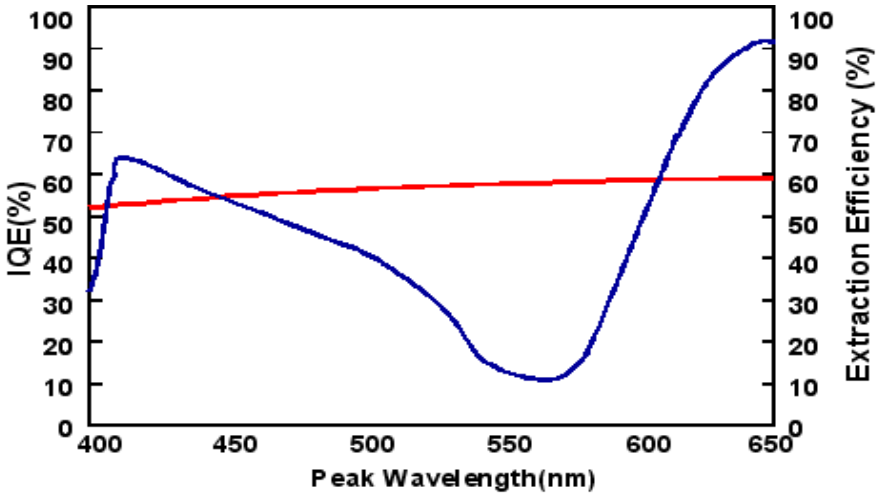
η_{int} : 내부양자효율 V_f : 순방향전압

η_{extr} : 적출효율 q : 전하량

- **Internal Efficiency**
  - ➢ 직접 천이형 반도체의 박막 성장과 고품위 양자우물구조를 이용한 Heterogeneous 구조 성장
  - ➢ Efficiency droop → Auger 비발광 재결합, Carrier 주입효율 악화



농도와 이동도가 상대적으로 작은 정공은 동작전압이 증가할수록 활성층 내부로 충분히 주입되지 못하는 반면 농도와 이동도가 큰 전자는 활성층 외부로 전자의 누설이 가속되고 결과적으로 누설 전류에 의한 p형 반도체 층에서의 비발광성 재결합 발생



04 Epi. / Chip Fabrication

Efficiency

외부양자효율 ∝ 전광변환효율

- **Wall Plug Efficiency**

$$\eta_{w\,PE} = \frac{P}{IV} = \frac{\text{광학적 출력}}{\text{전기적 입력}} \qquad \eta_{E\,QE} = \frac{P/(h\nu)}{I/e} = \frac{\text{자유공간으로 방출되는 광자수}}{\text{LED로 주입되는 전자수}}$$

- **내부양자효율 (Internal Quantum Efficiency, IQE)**

$$\eta_{int} = \frac{P_{int}/(h\nu)}{I/e} = \frac{\text{활성영역에서 방출된 광자수}}{\text{주입전자수}}$$

- **주입효율**

$$\eta_{inj} = \frac{I_{active}/e}{I_{applied}/e} = \frac{\text{활성영역 주입전류}}{\text{외부주입전류}}$$

- **적출효율**

$$\eta_{extraction} = \frac{P_{ex}/(h\nu)}{P_{int}/(h\nu)} = \frac{LED\text{외부로 방출 된 광자 수}}{\text{활성영역에서 방출된 광자수}}$$

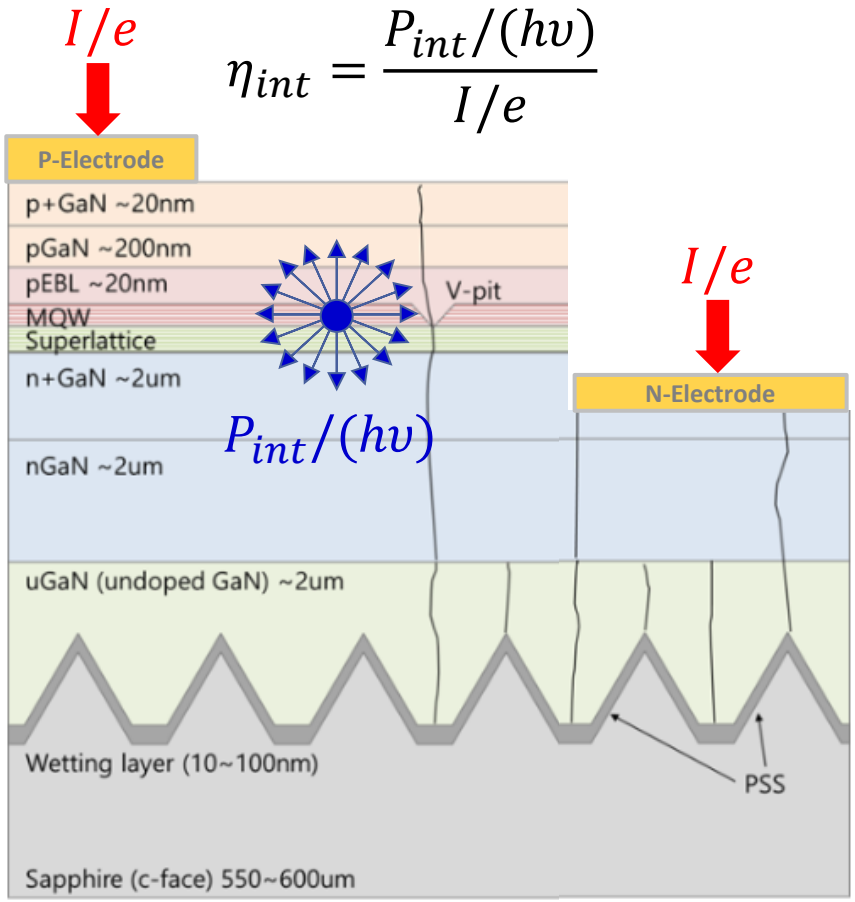
04 Epi. / Chip Fabrication

Efficiency

내부양자 효율

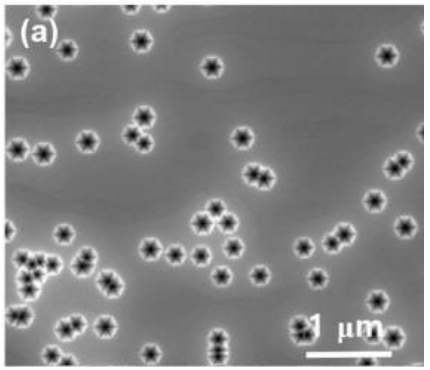
- Epitaxial

$$\eta_{int} = \frac{P_{int}/(h\nu)}{I/e}$$

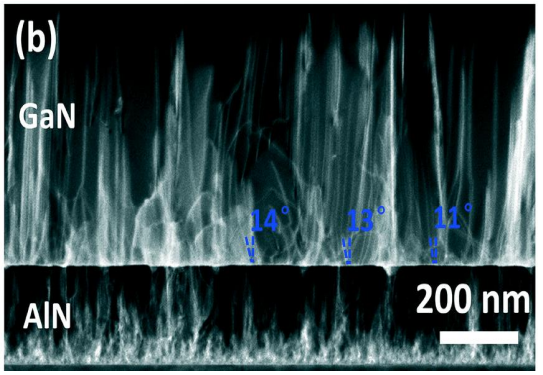


- MOCVD 장비 내 200개 층 형성 공정 (6 ~8 시간)
- 공정 온도 / 압력 : 550~1100℃, 70~600mBar
- 130개 이상 밸브와 장치 조정, 다양한 기체, 고체, 액체 소스(source)를 적용

[Surface Defect]



[Dislocation]

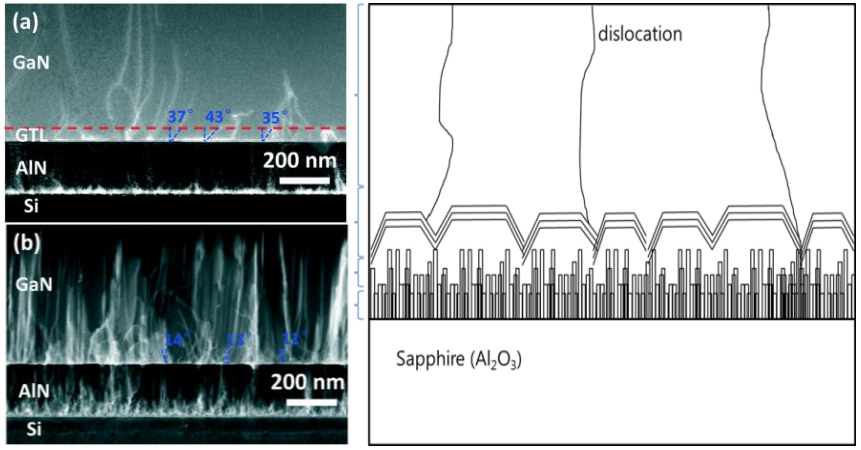


04 Epi. / Chip Fabrication

Efficiency

Defect & Dislocation

[Dislocation & Thread Defect]

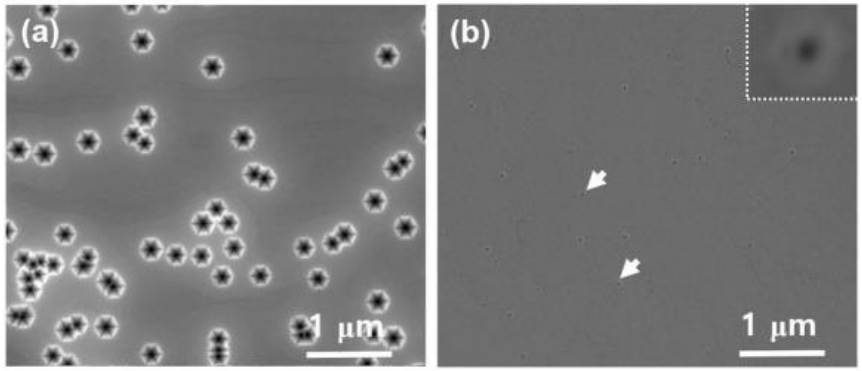


LED dislocation density : > 10^8/cm²

High Quality Epi. → Material Issue ⇩ MOCVD+HVPE+MBE → New Equipment

Micro/Nano LED dislocation density : < 10^5 ~ 10^6/cm² (1EA / 1 um pixel → 10^4/cm²)

[Surface Defect]



LED defect density : > 10 EA/cm²

Wafer Topological Defect → GaN Template ⇩ Epi. Thickness < 3 um → GaN Template

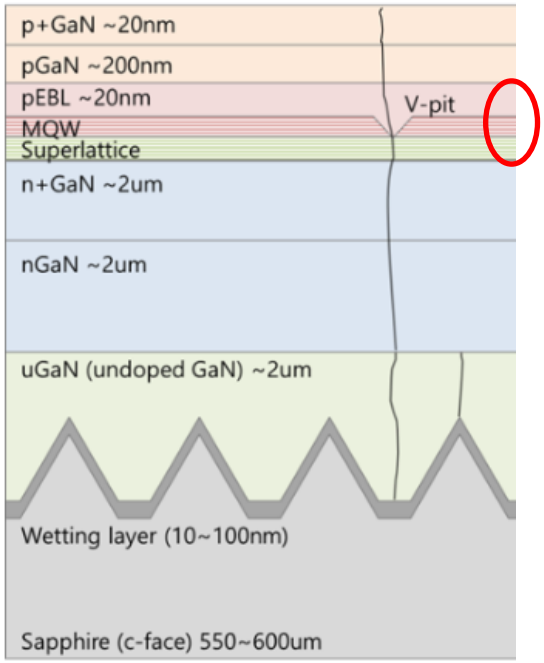
Micro/Nano LED Defec density : < 0.1EA/cm²

04 Epi. / Chip Fabrication

Efficiency

내부양자 효율

- **Efficiency Droop : the reduction of efficiency with increasing current or temperature(thermal droop)**
  - ➢ Two of the most recognized mechanisms are poor hole injection efficiency, Auger recombination and carrier leakage and the efficiency droop in c-plane GaInN/GaN LEDs is exacerbated due to the polarization effect.
  - ➢ To solve this issue, very low-droop blue GaInN/GaN LEDs have been realized on semipolar and nonpolar GaN substrates with reduced or eliminated polarization effects.



Surface Defect

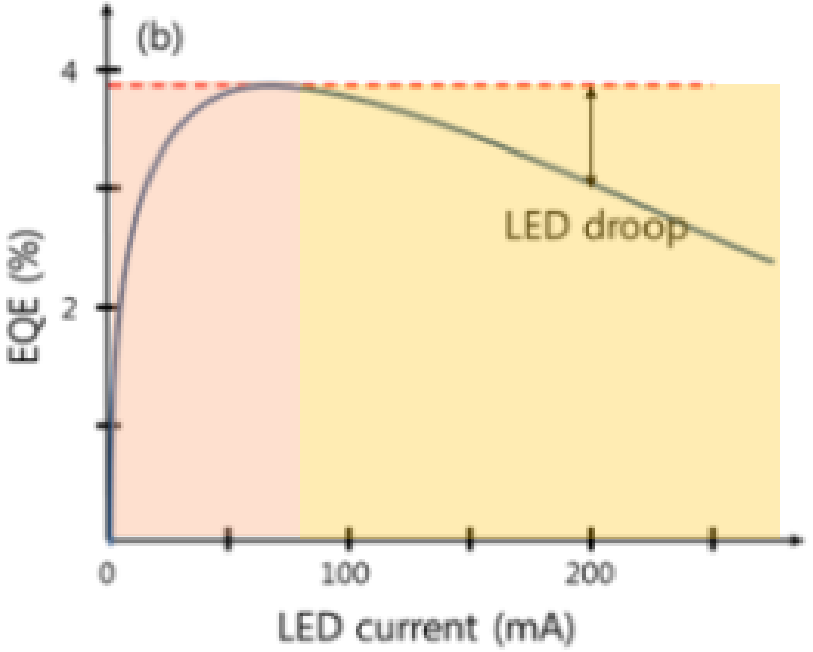
Carrier Overflow
Polarization
- QCSE
- Non-radiative recombination

MQW Defect
Auger recombination

Point Defect
Dislocation

Thread Dislocation

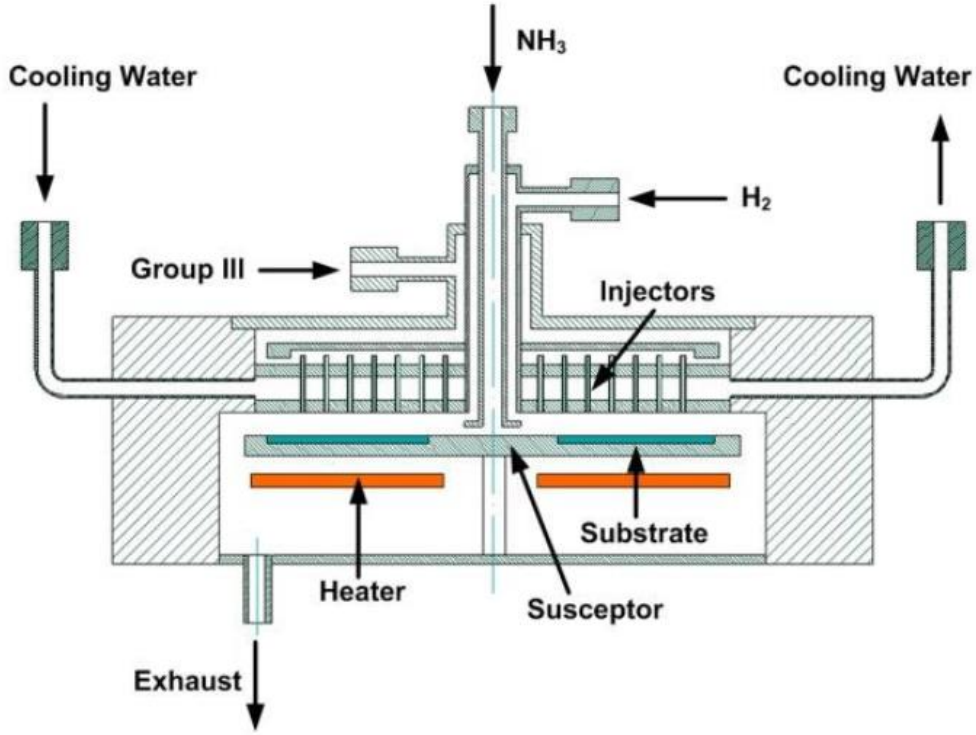
Topological Defect

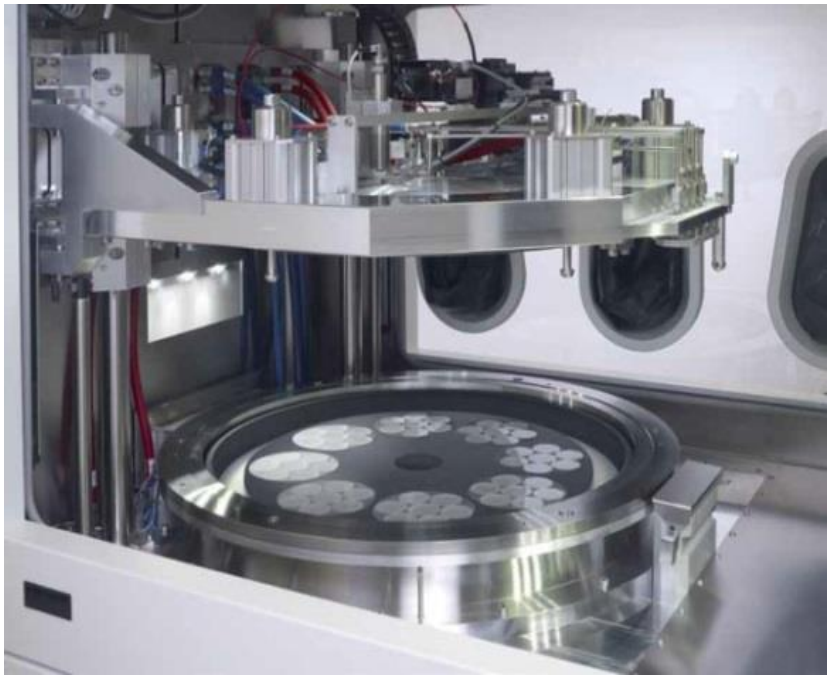


04 Epi. / Chip Fabrication

Efficiency

- **MOCVD (Metal organic Chemical Vapor Deposition)**





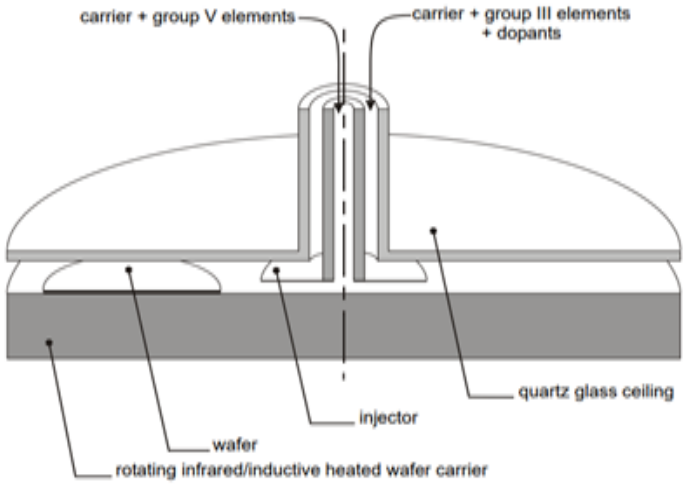
04 Epi. / Chip Fabrication

Efficiency

MOCVD (Metal organic Chemical Vapor Deposition)

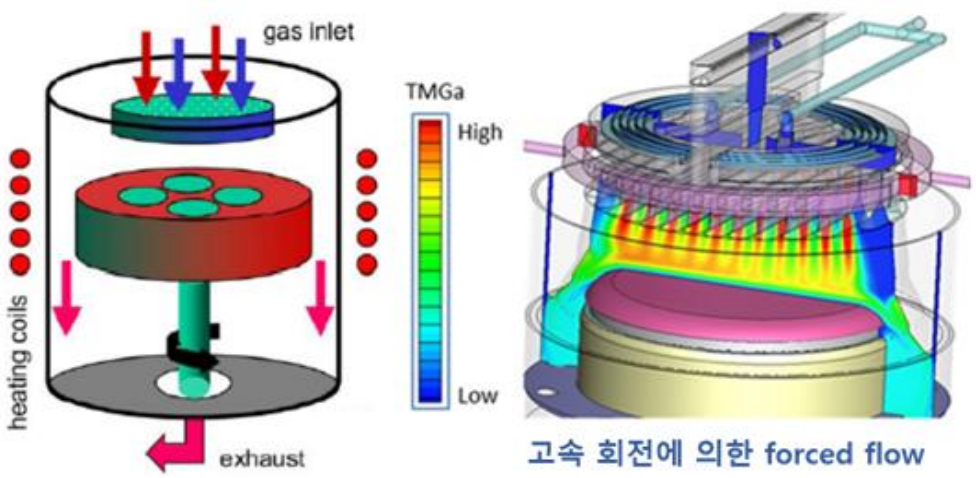
- **Plenetary Type (Hybrid) Vs Barrel Type (Vertical)**

[Planetary 타입 챔버]



- 수직 주입 - 수평 가스 Laminar Flow 확산 성장
- 에피 웨이퍼 uniformity 우수

[Barrel 타입 챔버]

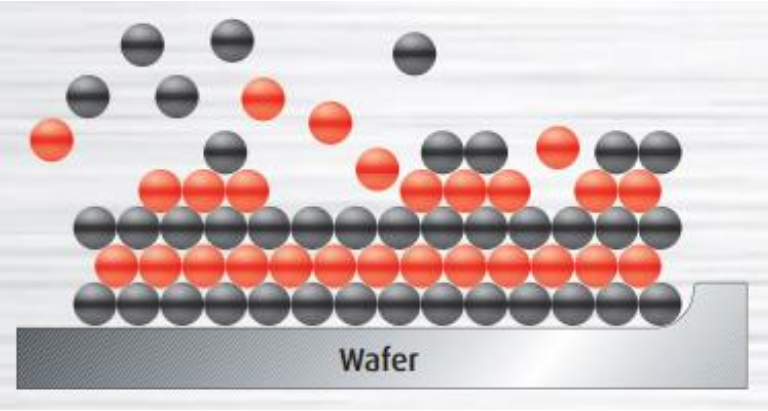


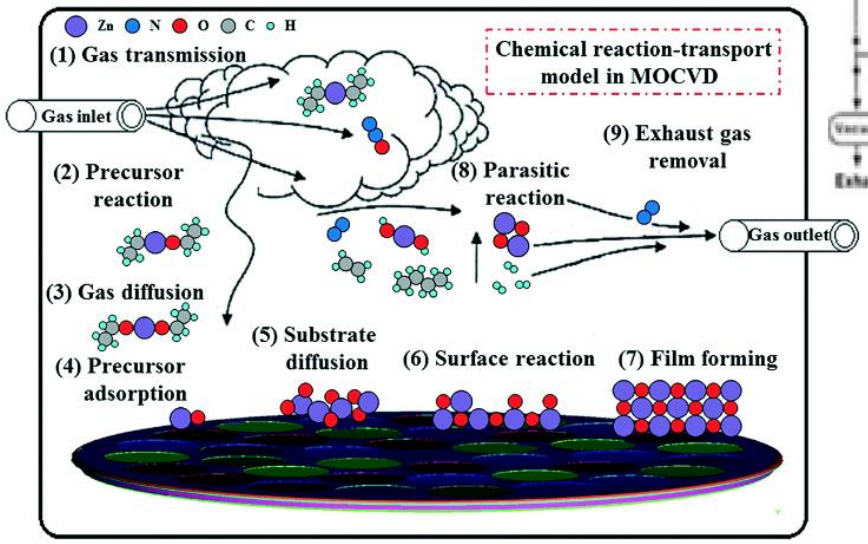
- 수직 주입 Forced Flow 성장
- 활성층 영역의 전구체 주입이 우수

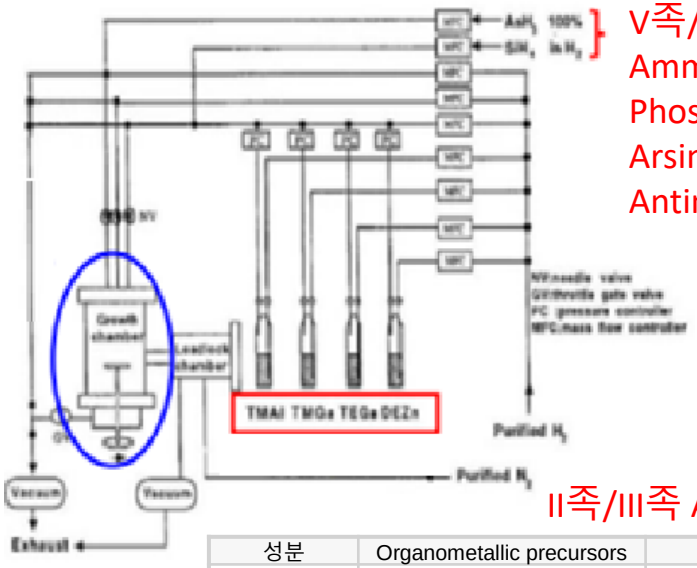
04 Epi. / Chip Fabrication

Efficiency

MOCVD (Metal organic Chemical Vapor Deposition)







V족/VI족 Hybrid Source
Ammonia NH3, Gas
Phosphine PH3, Gas
Arsine AsH3, Gas
Antimony Stibine SbH3, Gas

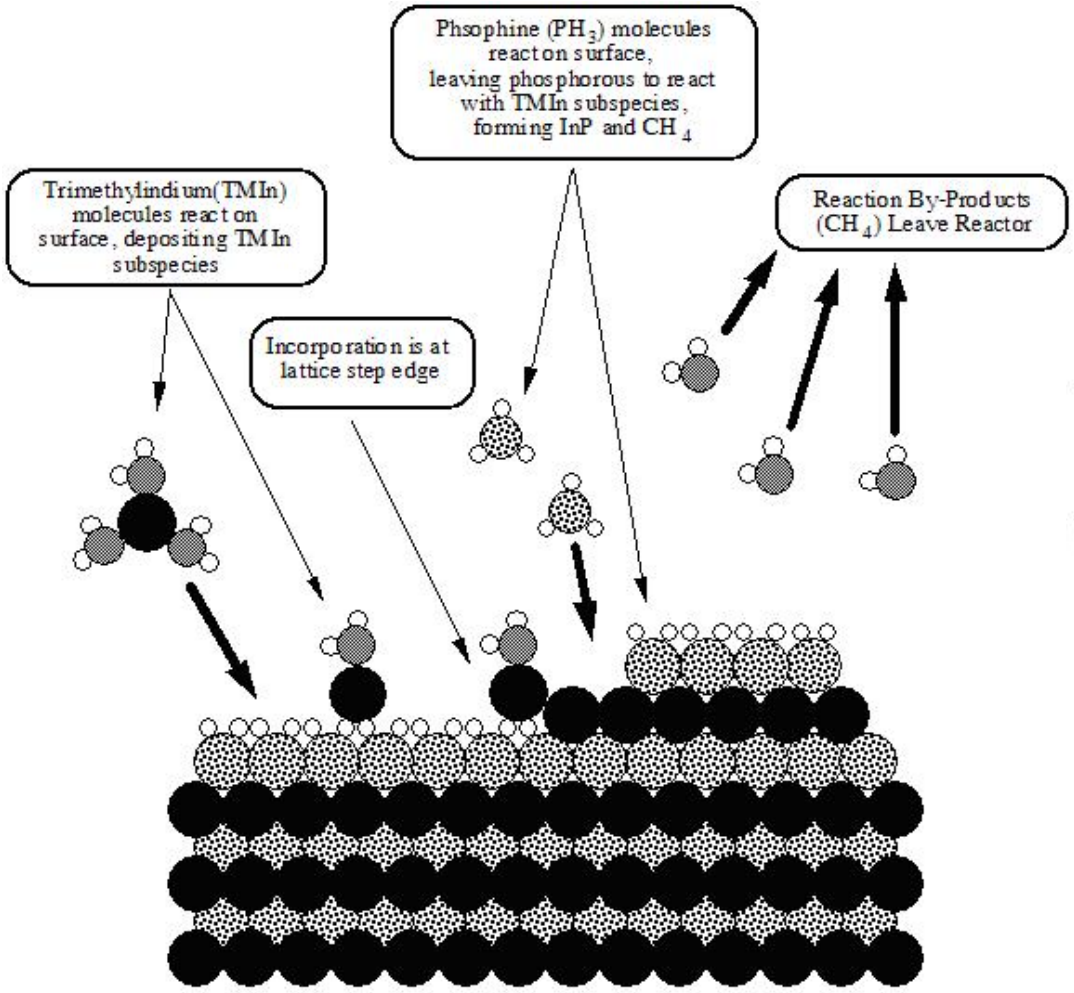
II족/III족 Alkyl Source

성분	Organometallic precursors	약어	성상	구성
Aluminium	Trimethylaluminium	TMA or TMAl	Liquid	C6H18Al2
	Triethylaluminium	TEA or TEAl	Liquid	C12H30Al2
Gallium	Trimethylgallium	TMG or TMGa	Liquid	Ga(CH3)3
	Triethylgallium	TEG or TEGa	Liquid	C6H15Ga
Indium	Trimethylindium	TMI or TMIn	Solid	C3H9In
	Triethylindium	TEI or TEIn	Liquid	C6H15In
Magnesium	bis(cyclopentadienyl) Mg	Cp2Mg	Solid	Mg(C5H5)2
Zinc	Dimethylzinc	DMZ	Liquid	Zn(CH3)2
	Diethylzinc	DEZ	Liquid	(C2H5)2Zn

04 Epi. / Chip Fabrication

Efficiency

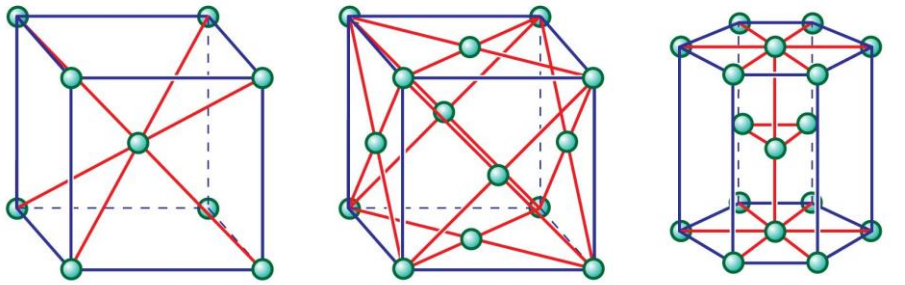
MOCVD (Metal organic Chemical Vapor Deposition)



Mismatch	Si	SiC
Crystal Structure	FCC	HCP
Lattice Constant (Å)	5.43	3.08
Lattice Mismatch (%)	−16.9	3.5
Thermal Expansion (10^{-6} K)	3.59	4.3
Thermal Mismatch (%)	55	30

Mismatch	Sapphire	AlN	GaN
Crystal Structure	HCP	HCP	HCP
Lattice Constant (Å)	4.758	3.112	3.189
Lattice Mismatch (%)	16.08	2.4	-
Thermal Expansion (10^{-6} K)	7.3	4.15	5.59
Thermal Mismatch (%)	−23	34	-

Common metallic crystal structures



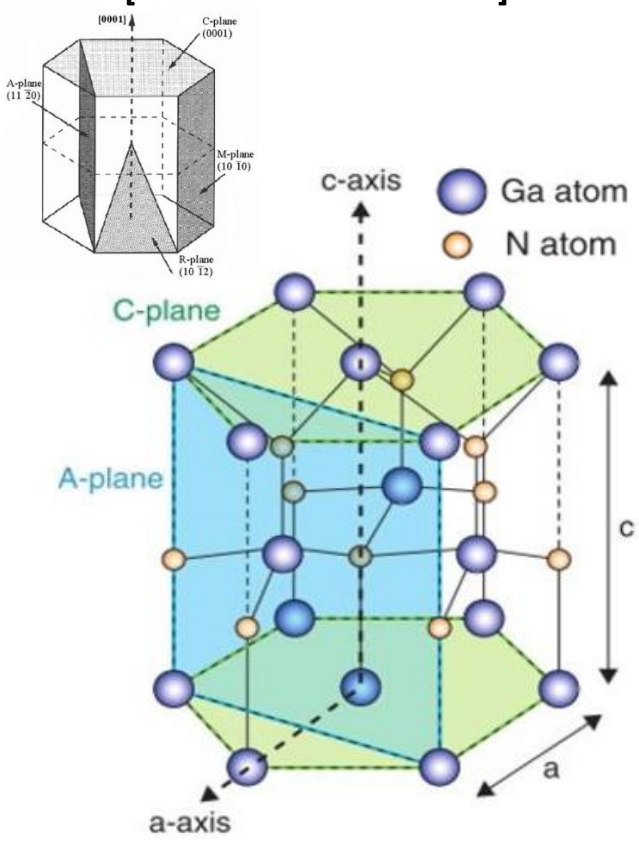
body-centred cubic (bcc) face-centred cubic (fcc) hexagonal close-packed (hcp)

04 Epi. / Chip Fabrication

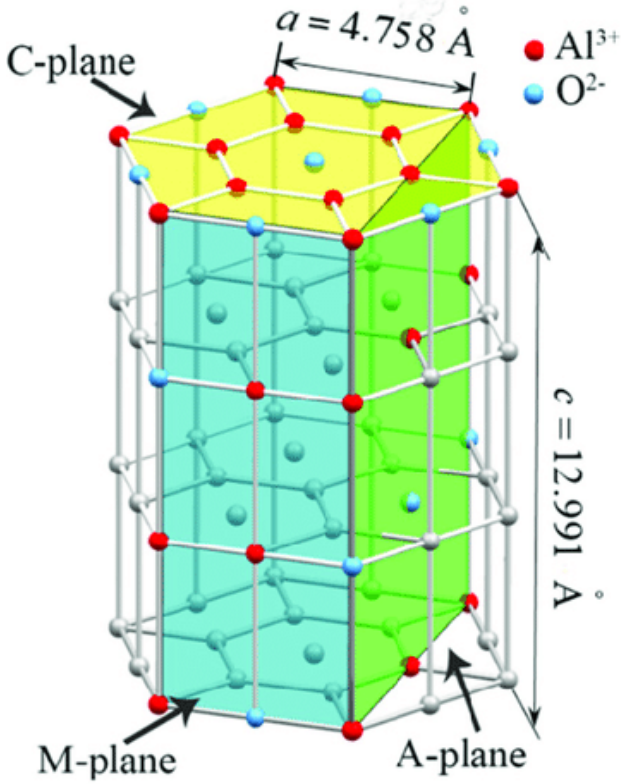
Efficiency

Lattice Structure

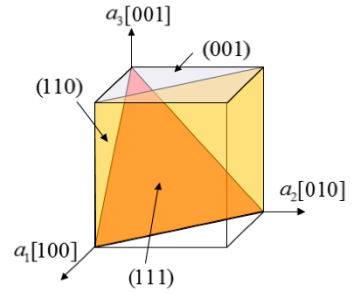
[GaN 0001 axis C-Plane]

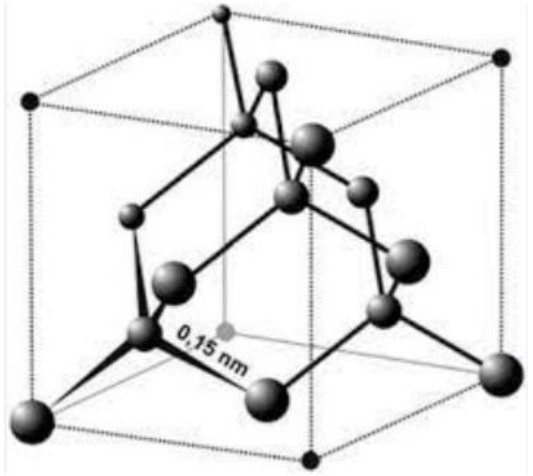


[Sapphire 0001 axis C-Plane]



[Si 111 axis]

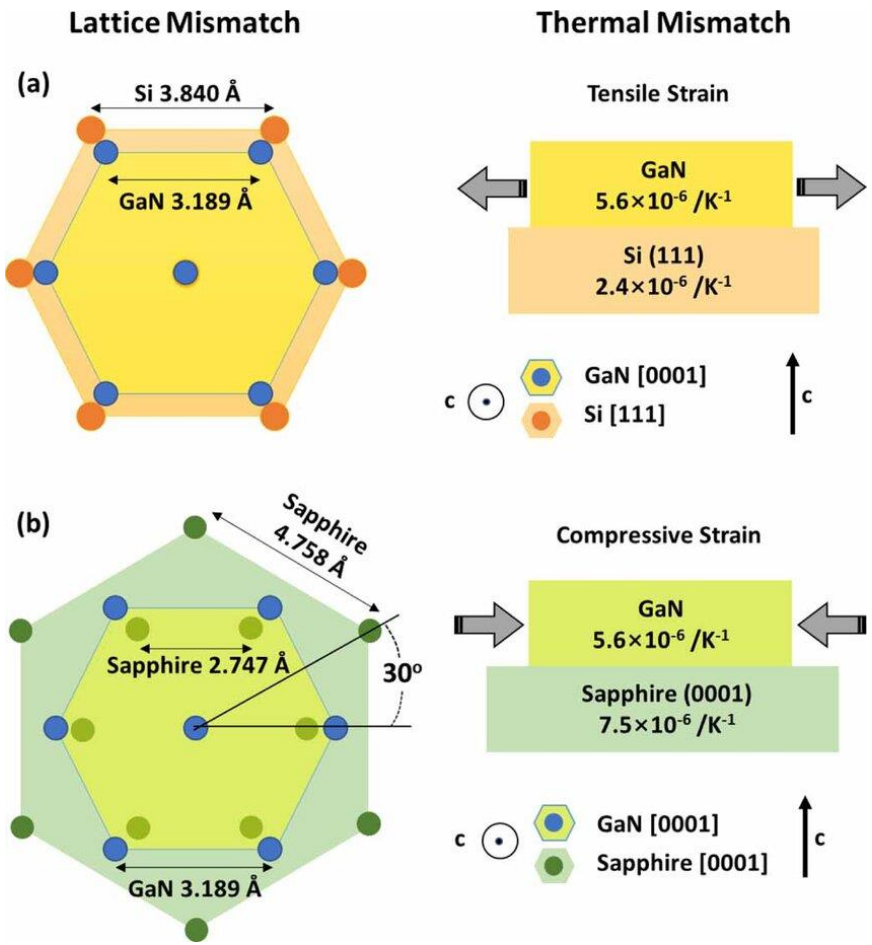


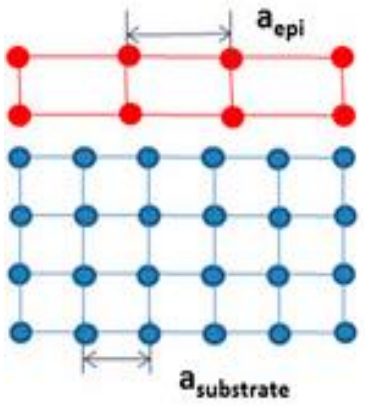


04 Epi. / Chip Fabrication

Efficiency

Lattice Structure



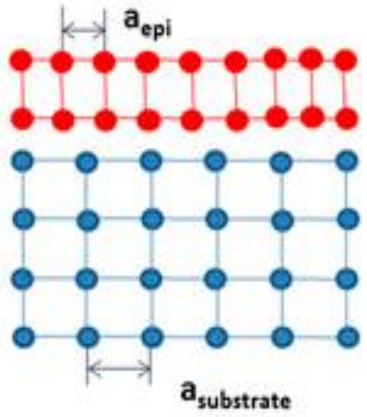


$a_{epi} > a_{substrate}$

or $CTE_{epi} < CTE_{substrate}$

Convex

Compressive in epi



$a_{epi} < a_{substrate}$

or $CTE_{epi} > CTE_{substrate}$

Concave

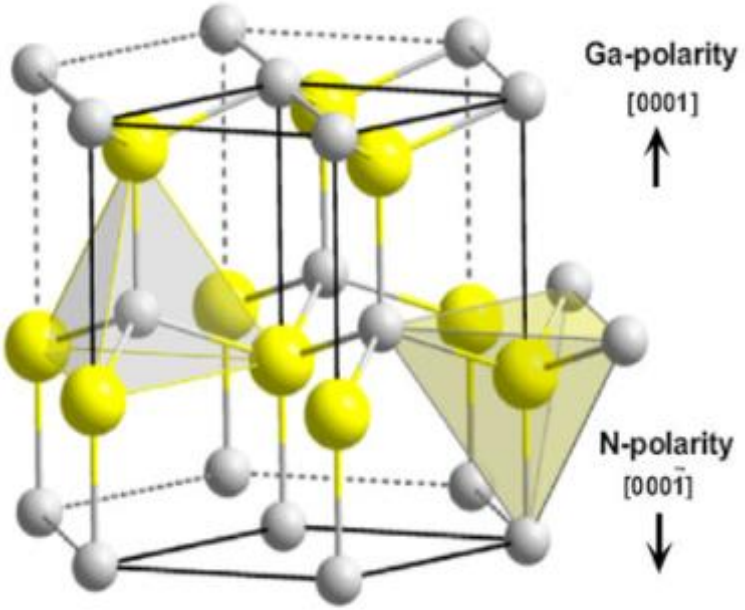
Tensile in epi

04 Epi. / Chip Fabrication

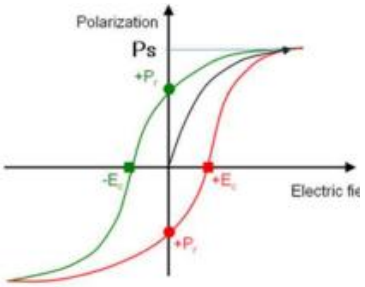
Efficiency

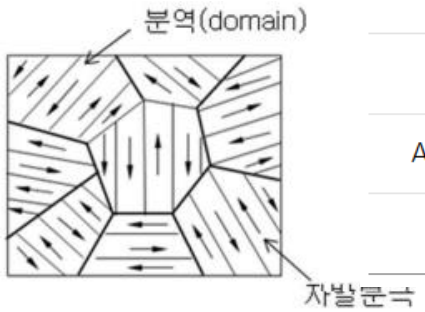
Polarization & Electric Field

- 우르자이트(Wurzite) 결정구조의 GaN은 사파이어 c면의 수직인 c축에 우선 배향된 형태로 성장
- c축 방향을 따라 위쪽은 Ga 원자, 아래쪽은 N 원자가 위치, 평형상태 (Electric Field가 0)에서도 자발적인 분극(Spontaneous Polarization)이 발생



GaN의 Wurtzite 결정 구조도





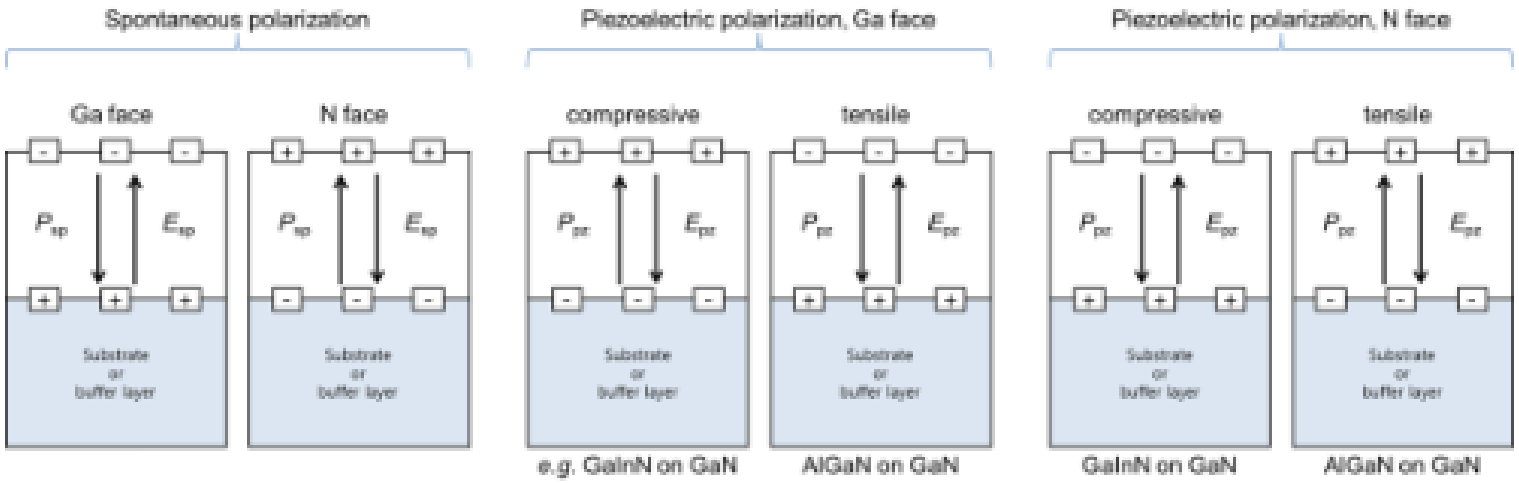
	a(Å)	c(Å)	αa(10-6K-1)	αc(10-6K-1)
GaN	3.189	5.185	5.59	3.17
AlN	3.111	4.98	5.3	4.2
Al2O3	4.758	12.99	7.5	8.5
InN	3.545	5.703	5.7	3.7

04 Epi. / Chip Fabrication

Efficiency

Polarization & Electric Field

- 격자 내 서로 다른 원자 간 자발분극 및 압전분극에 의한 내부전계, 전류 주입에 따른 외부 전계에 의해 응력이 발생하게 되고, 이로 인한 격자 간 변형에 다른 압전 분극 효과 발생
- 기계적 응력이 격자 내의 전하 변위를 발생시킬 수 있으나, 격자 간 대칭성을 갖고 있으면 압전 분극은 발생하지 않음



C축으로 성장된 GaN의 경우 Ga면을 가지며, Ga면-N면의 분극장과 전계는 서로 반대 방향으로 자발 극성이 나타나게 남

InGaN/GaN (활성층, SPSL), AlGaN(EBL)/GaN 사이에 자발 분극 극성에 따른 압전 분극이 발생

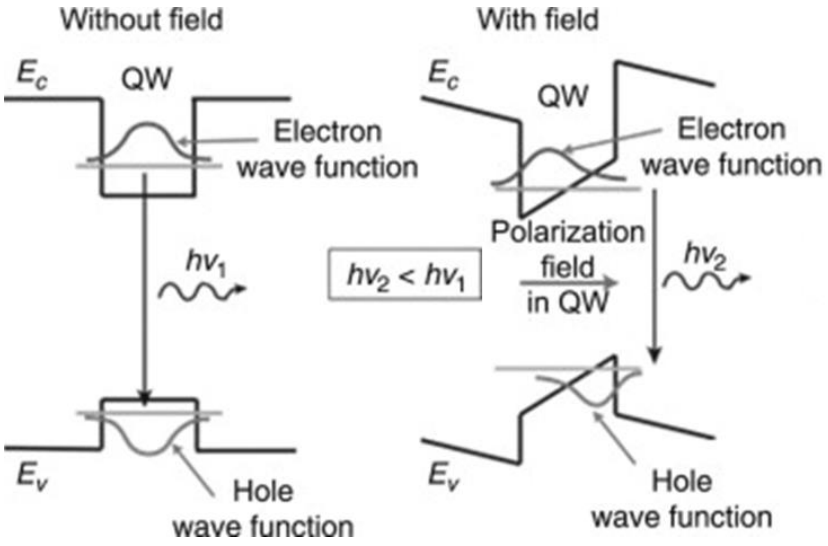
→ LED 내의 압전분극, 열에 의한 외력(Stress)에 따른 격자변형/부정합 (Strain)은 전기장 (Electric Field) 을 변화시키게 되고, 이로 인한 에너지 밴드구조의 변화와 전자-전공의 분포 및 파동함수에 영향을 주게 됨(MQW로의 Carrier Generation 및 Recombination에 직접적인 영향 요소)

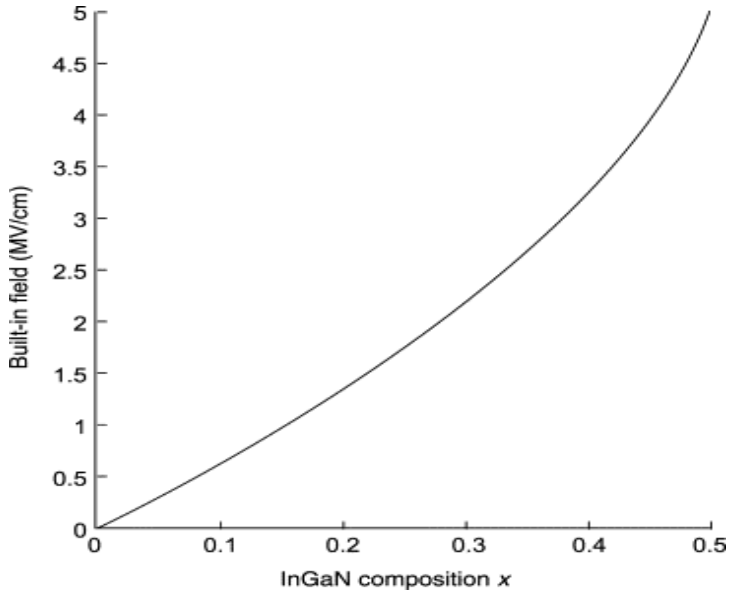
04 Epi. / Chip Fabrication

Efficiency

Polarization & Electric Field

- **Usually the barrier and QW regions have different polarization values, producing a discontinuity at the heterointerface. The polarization discontinuity manifests as a bound interface charge, which density is usually of the order of 10^{13} cm^{-2} resulting in large electric fields in the quantum well of the order of ~ MV/cm**
- **Quantum Confined Stark Effect (QCSE) → Reduction of IQE, Increase of threshold voltage**
  - ➢ The polarization-induced field in the QW reduces the transition energy from the first electron subband to the first hole subband resulting in a red-shift of the emission





Takeuchi *et. al.*, 1997; Deguchi *et. al.*, 1999, https://www.sciencedirect.com/topics/chemistry/quantum-confined-stark-effect

04 Epi. / Chip Fabrication

Efficiency

Polarization & Electric Field

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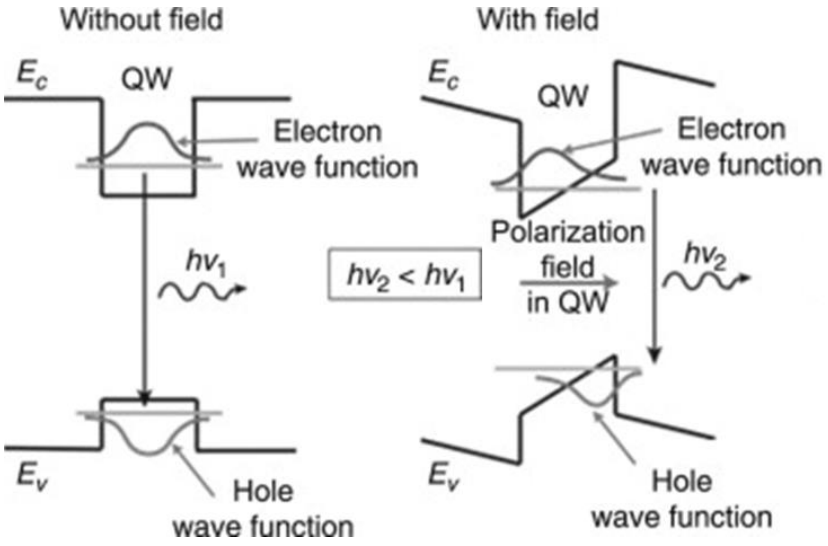
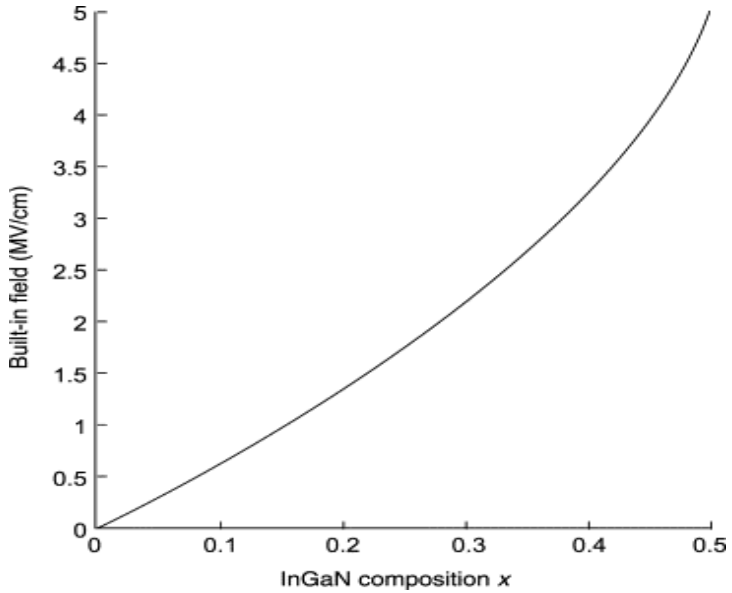




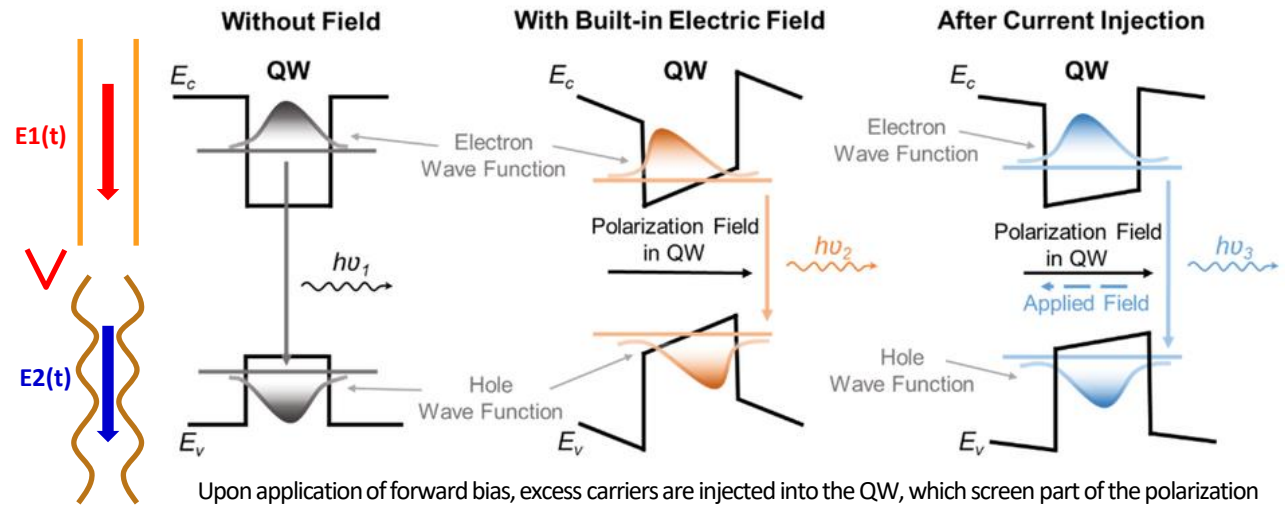
Takeuchi *et. al.*, 1997; Deguchi *et. al.*, 1999, https://www.sciencedirect.com/topics/chemistry/quantum-confined-stark-effect

04 Epi. / Chip Fabrication

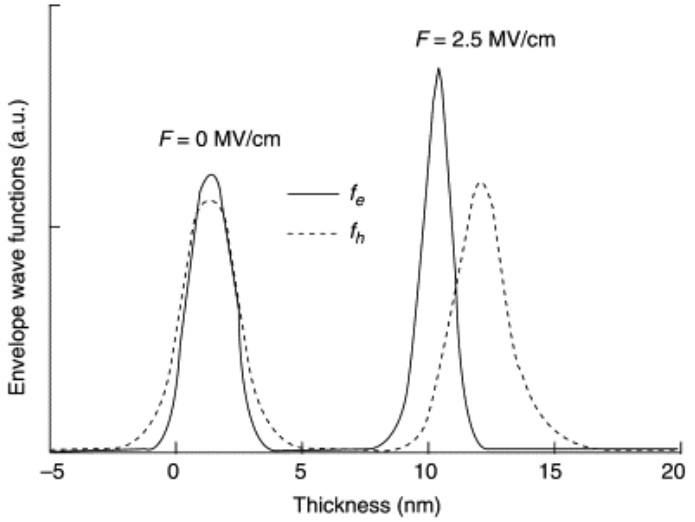
Efficiency

내부양자효율 : Polarization & Electric Field

- **Oscillation strength of polarization & electric filed**
  - The rate at which an electron in the conduction band state |c〉 relaxes to an empty state (hole) in the valence band |v〉 by emitting a photon is given by Fermi's golden rule for optical transitions
  - The optical radiative transition rate is proportional to the strength of the interaction between the electron and photon systems.
  - The spatial separation of electron and hole envelope functions due to the field in the QW reduces the radiative recombination rate, thus allowing non-radiative processes an upper hand in the competition for carrier recombination, leading to reduced IQE of light-emitting devices.



Upon application of forward bias, excess carriers are injected into the QW, which screen part of the polarization field, leading to blue-shifting of the spectrum with increasing current density



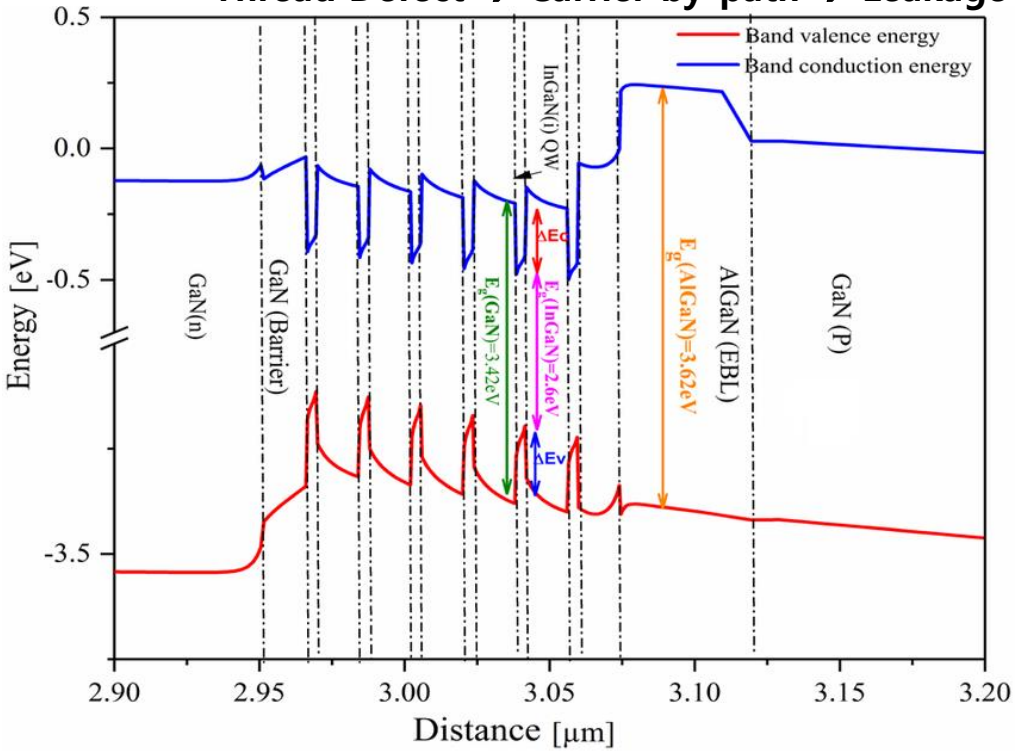
Im et al., 1998, https://www.sciencedirect.com/topics/chemistry/quantum-confined-stark-effect

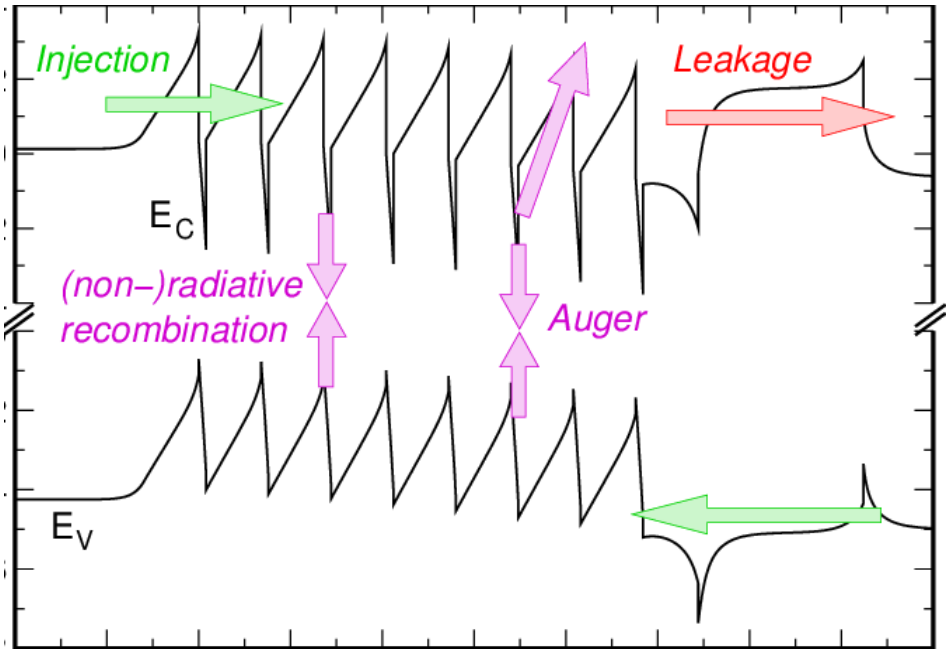
04 Epi. / Chip Fabrication

Efficiency

Multi-Quantum Well

- Non radiative recombination : At a side of the edge, partially filled electron orbitals, or dangling bonds, are electronic states that can be located in the forbidden gap
- Auger recombination : dissipated by the excitation of a free electron high into the conduction band, or by a hole deeply excited into the valence band.
- Thread Defect → Carrier by-path → Leakage Current



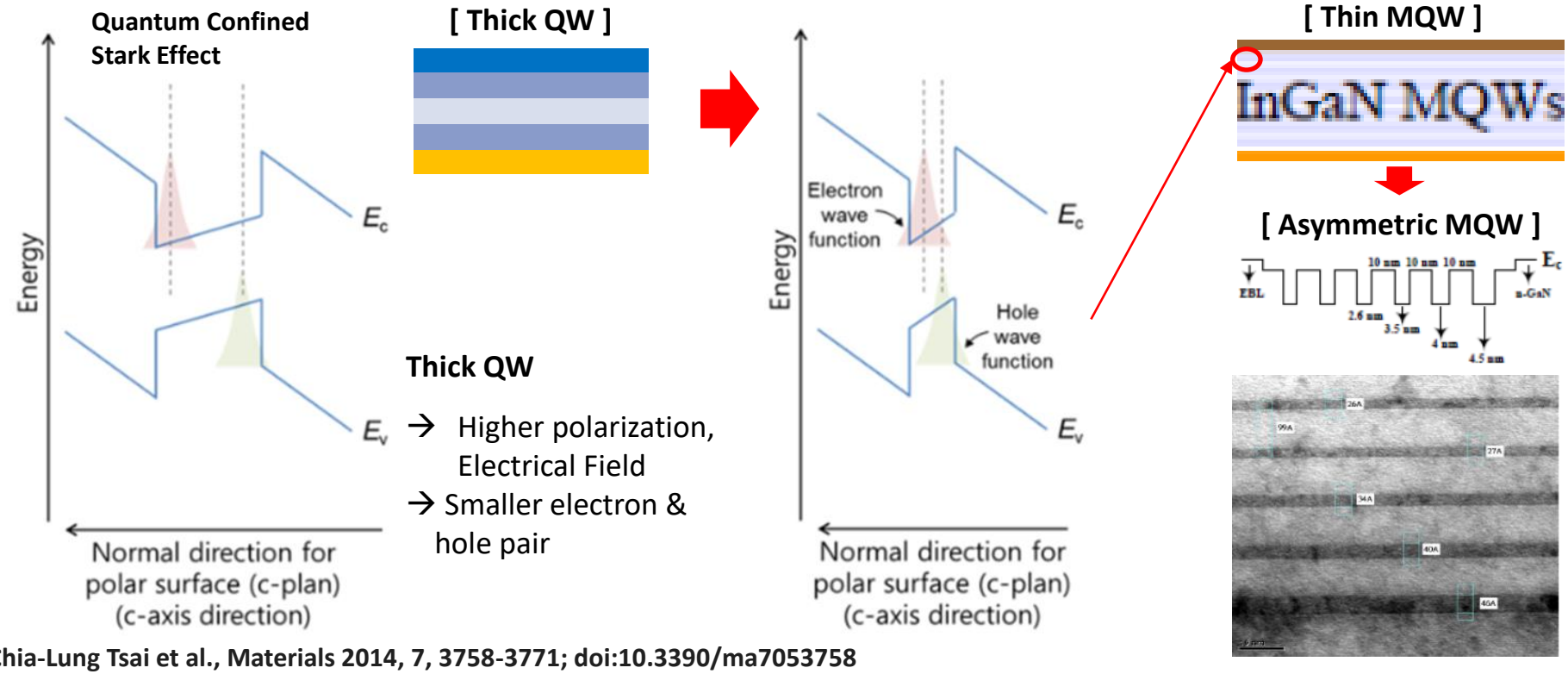


04 Epi. / Chip Fabrication

Efficiency

Multi-Quantum Well

- **Why multi-quantum well (MQW) ?**
  - ➢ Non-radiative recombination by non-linear electron & hole pair wave function → Narrow matching range → Thin multi GaN/InGaN well structure
  - ➢ Poor Hole Injection → AQW (**Asymmetric multi-Quantum Well) : 1st Well < 2nd Well < 3rd Well …**



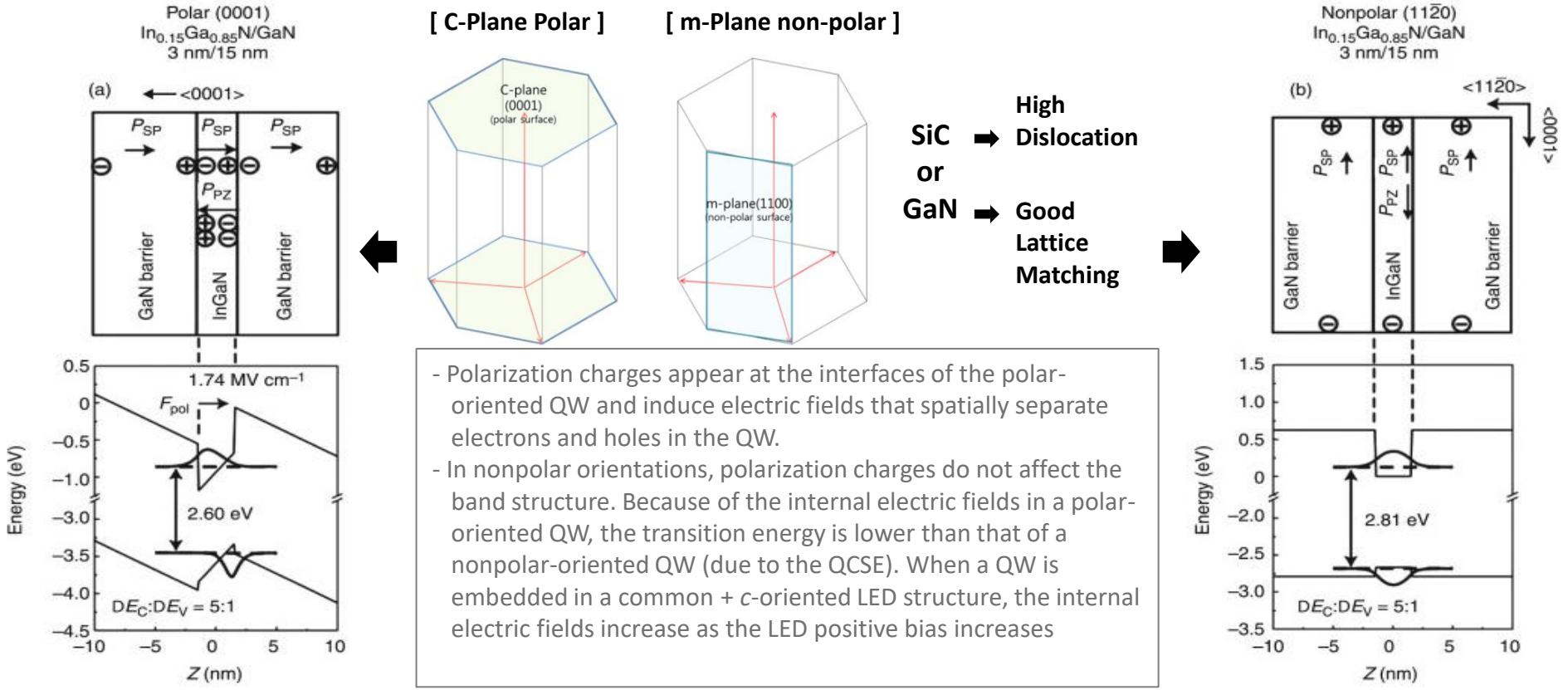
Chia-Lung Tsai et al., Materials 2014, 7, 3758-3771; doi:10.3390/ma7053758

04 Epi. / Chip Fabrication

Efficiency

Multi-Quantum Well

- **Reduction of the stress by polarization & electric field**
  - ➢ Epitaxy growth on m-Plane(non-polar) GaN template → less strain as lower stress between Ga and N atom → lower the simultaneous polarization and piezoelectric polarization



- Polarization charges appear at the interfaces of the polar-oriented QW and induce electric fields that spatially separate electrons and holes in the QW.
- In nonpolar orientations, polarization charges do not affect the band structure. Because of the internal electric fields in a polar-oriented QW, the transition energy is lower than that of a nonpolar-oriented QW (due to the QCSE). When a QW is embedded in a common + *c*-oriented LED structure, the internal electric fields increase as the LED positive bias increases

Chichibu *et al.*, 2006; Masui *et al.*, 2010

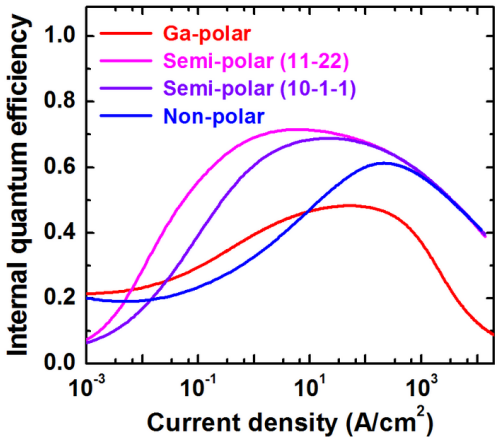
04 Epi. / Chip Fabrication

Efficiency

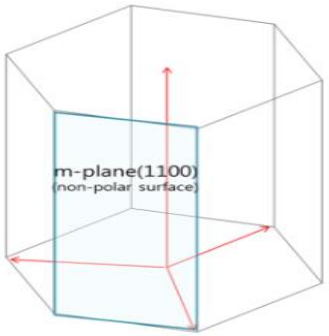
내부양자효율

: Polarization & Electric Field

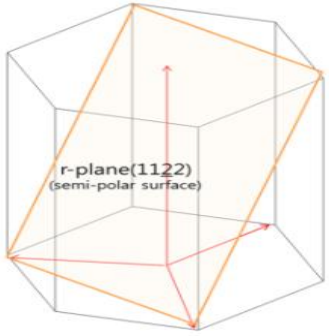
- It is seen that in the Ga-faced structure, there is a barrier hindering the electron injection into the MQW active region. Substantially lower barrier is formed in the non-polar and semi-polar structures
- The distributions of charge concentration in quantum wells of the non-polar and semi-polar structures are more homogeneous and recombination is more efficient



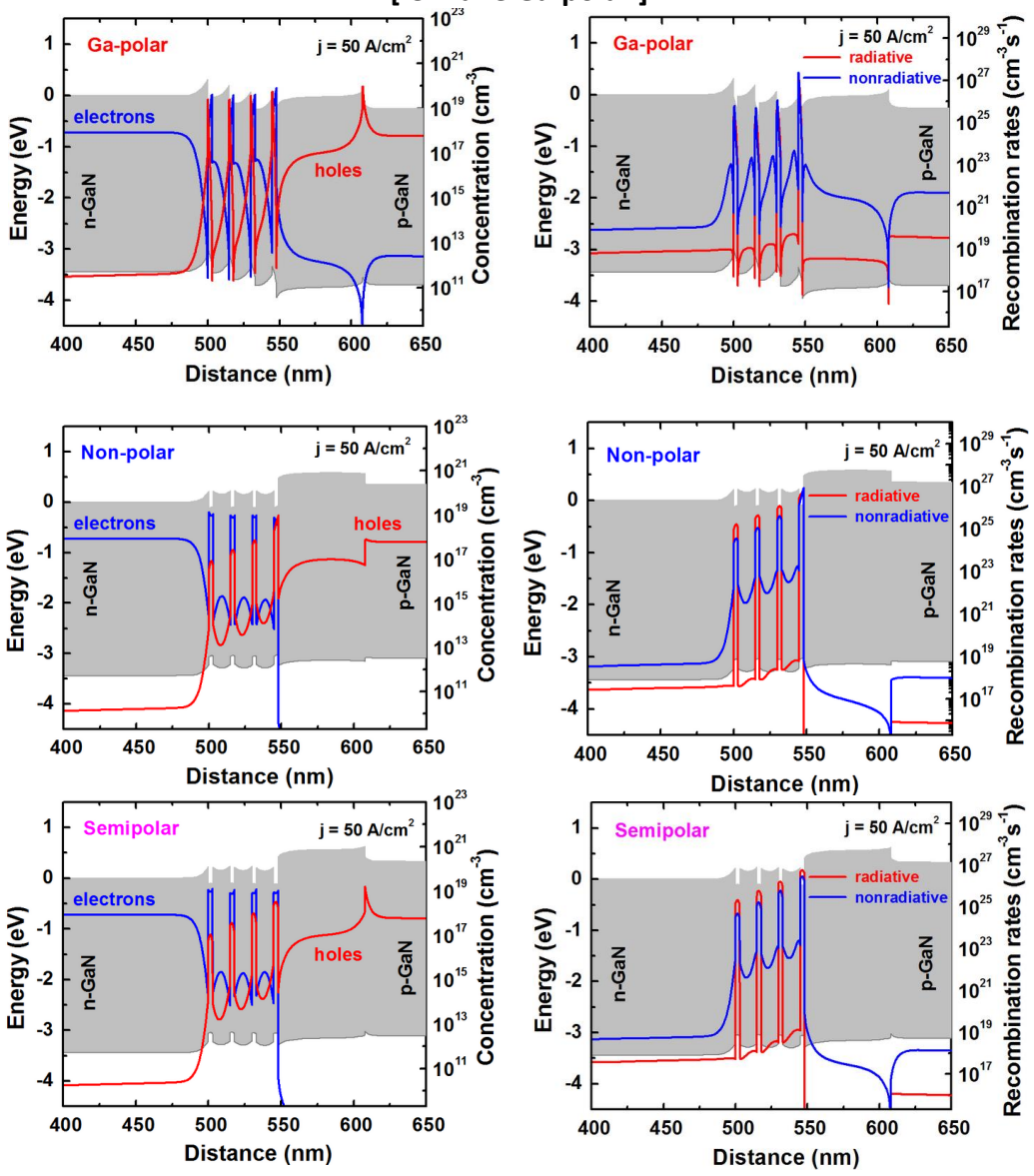
[m-Plane non-polar]



[r-Plane semi-polar]



[C-Plane Ga-polar]

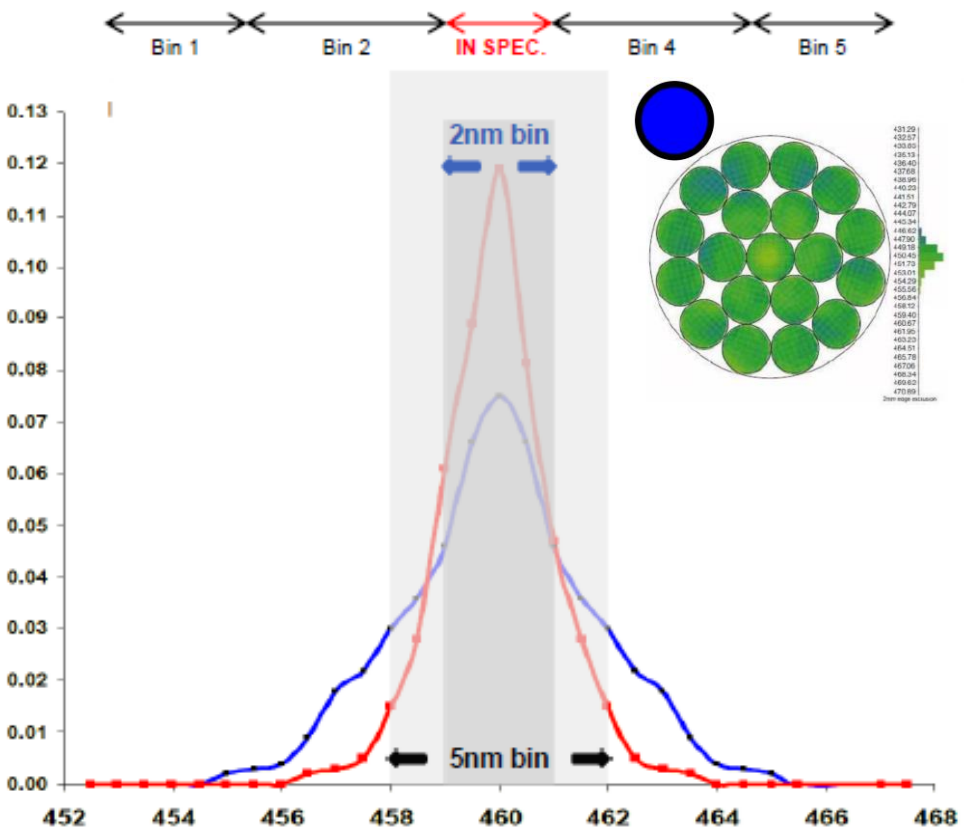


V.F. Mymrin, K.A. Bulashevich, N.I. Podolskaya and S.Yu. Karpov, Journal of Crystal Growth Volume 281, Issue 1, 15 July 2005, Pages 115-124.

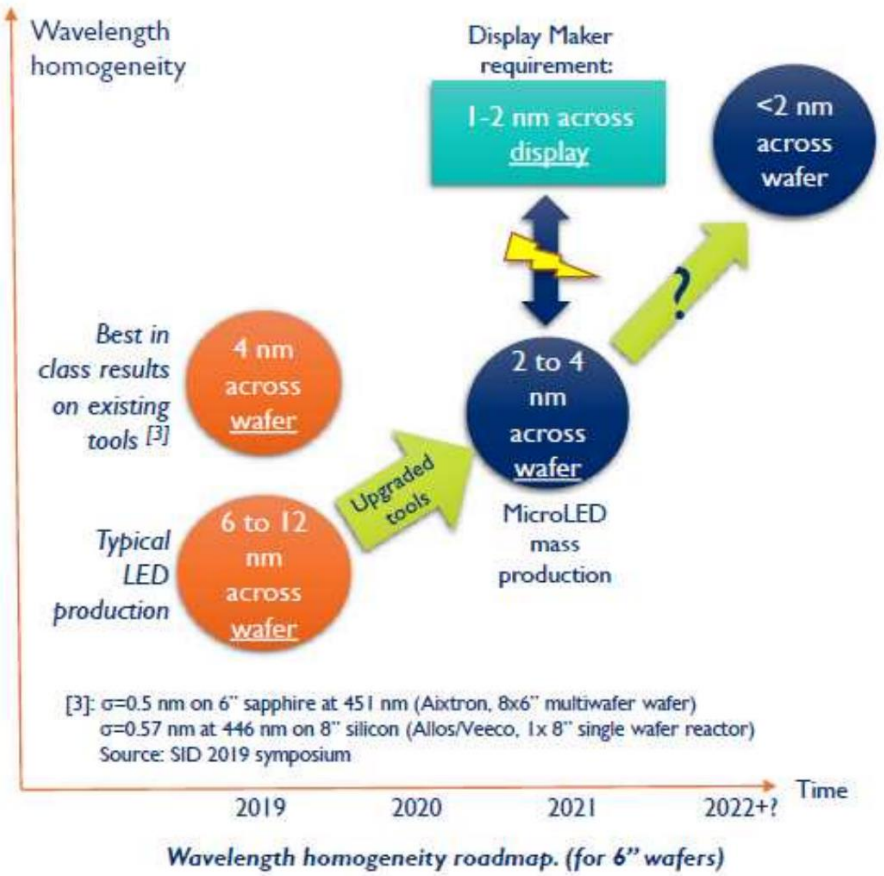
04 Epi. / Chip Fabrication

Current Status

Wavelength Uniformity



Wavelength binning distribution
Source: Veeco / Yole Développement



Wavelength homogeneity roadmap. (for 6" wafers)

04 Epi. / Chip Fabrication

Current Status

Wavelength homogeneity & Defects

Standard LED	µLED target	2022 Status [1]	
		On-wafer	Total [2]
6 to 12 nm	Red: < 3 nm	<1.5 nm	<2 nm
	Green: < 3-4 nm	<2.7 nm	<4 nm
	Blue: < 2-3 nm	<1.8 nm	<3 nm

The ultimate goal is a "1 bin" capability in 8" wafers to eliminate wavelength binning.

Standard LED	Requirements	2022 Status
0.5 to 10 cm^{-2} For defects > 2 µm	Application dependent: *< 0.1 to 0.02 cm^{-2} For defects > 0.2 to 1 µm*	≤ 0.1 cm^{-2} for particles > 0.3 µm;

0.2 µm defects could be killers.
For 1 µm or less size, It needs that over-specifying would increase epi-wafer cost.

	Substrate	Epi	CR Environment
Stains	X		X
Particles	X	X	X
Scratches	X		X
Pits, etc....	X	X	
Other defects		X	

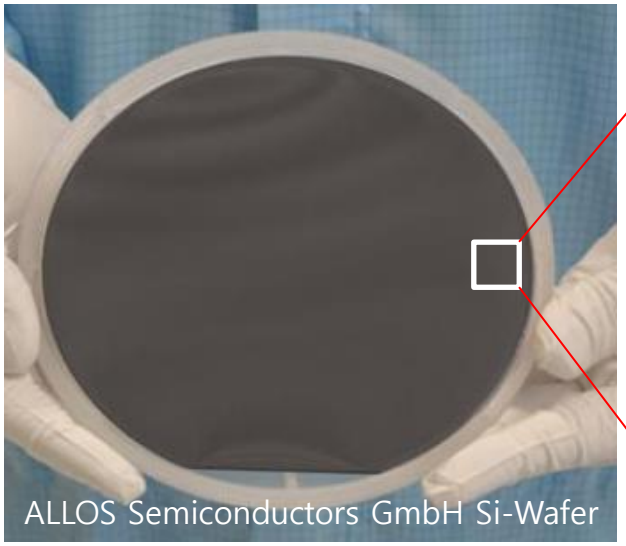
* Source : Yole Development, IDTech EX Research

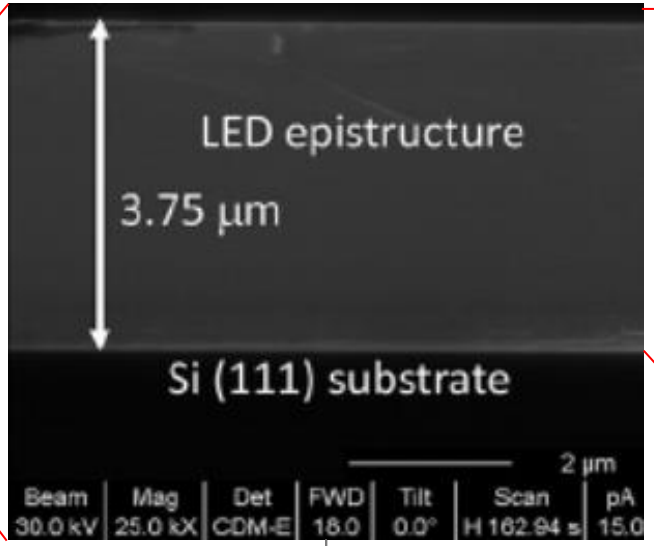
04 Epi. / Chip Fabrication

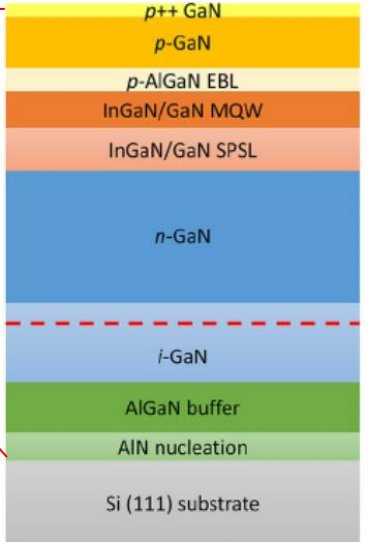
Material & Manufacturing Issues

- In standard LED production, defect densities fall into a 0.5-10/cm^2 range(1/cm^2 typicalin tier 1 fabs)
- Defect density for Micro LED can be brought down to the 0.1-0.15/cm^2 range

  → Defect size is 1/5th times smaller than conventional size about 1 um







Epi. Wafer Quality	Epi. Materials (Precursor)	Particles Control	Epi./Chip Equipment	Defect Inspection

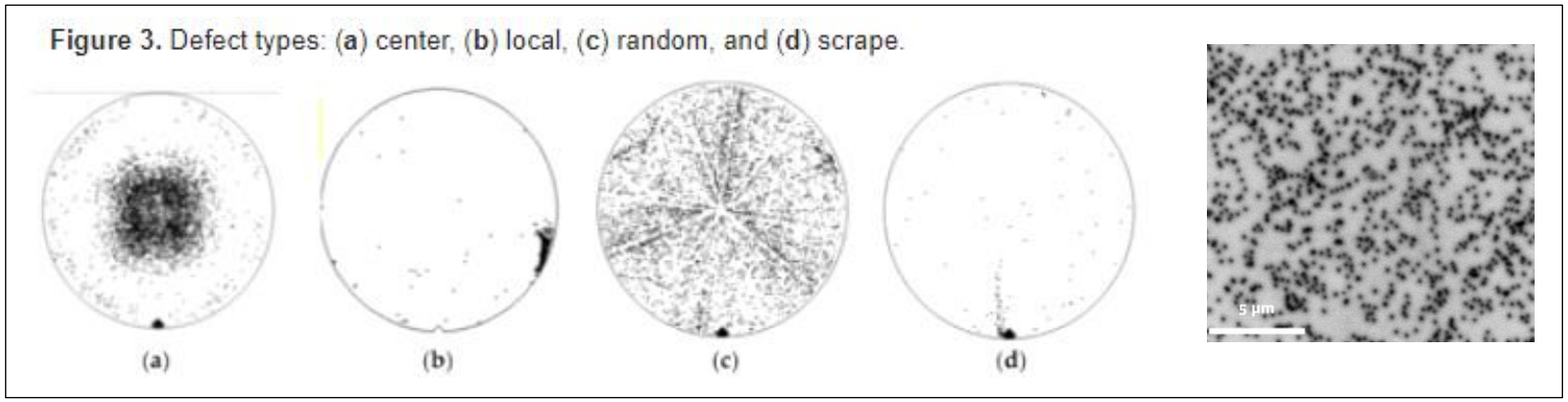
04 Epi. / Chip Fabrication

Wafer (Template) for epitaxial

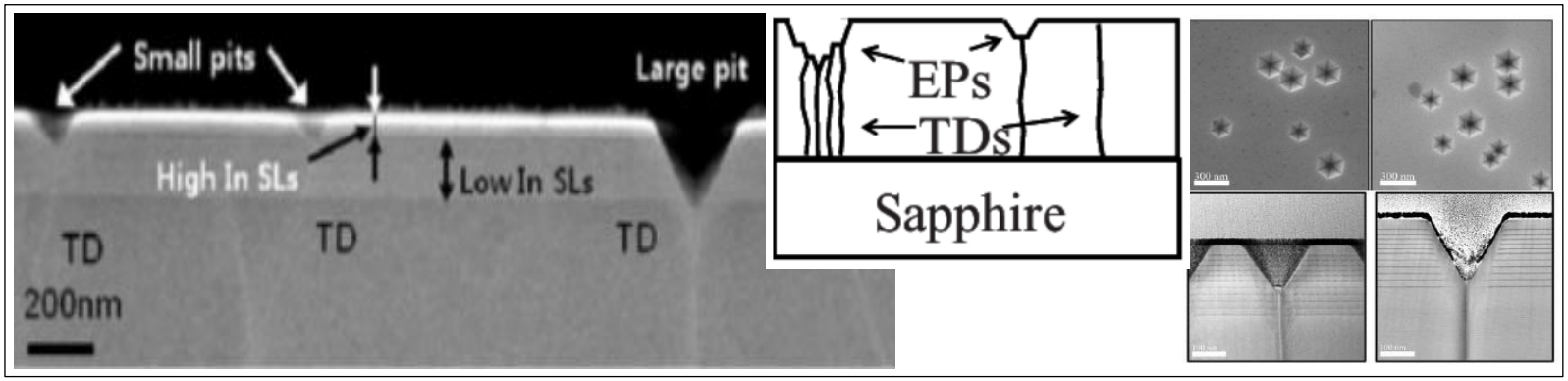
Wafer Defect → Epi. Defect → Dead Pixel

- Traditional LED Wafer optimized with typical dimensions ranging from 250 to more than1,000 µm not suitable for MicroLED

Epi. Wafer Quality



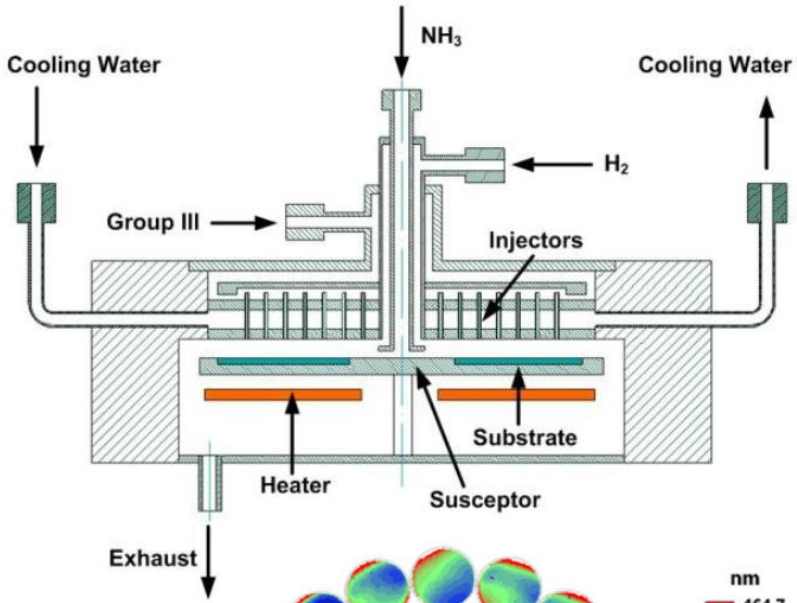
Epi. Defect

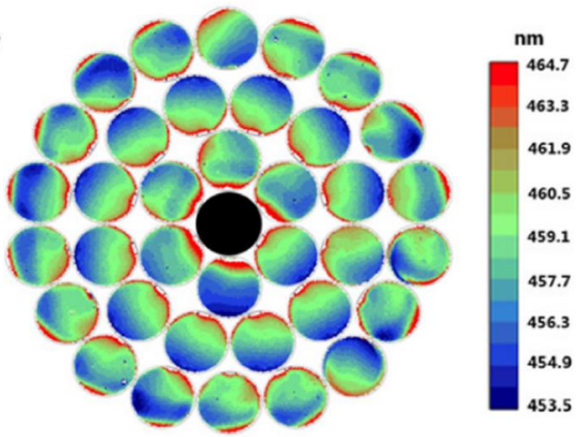


04 Epi. / Chip Fabrication

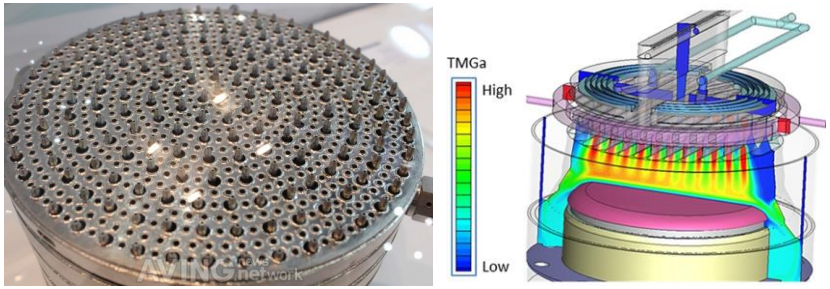
Epi. Equipment

MOCVD

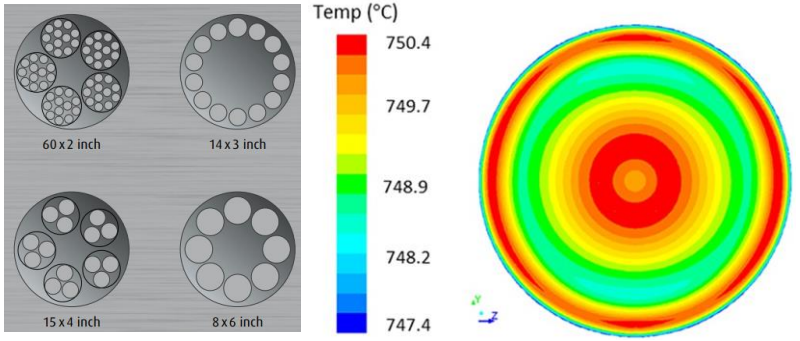


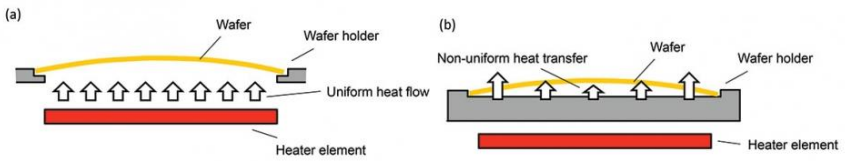


[Shower Head]



[Susceptor]





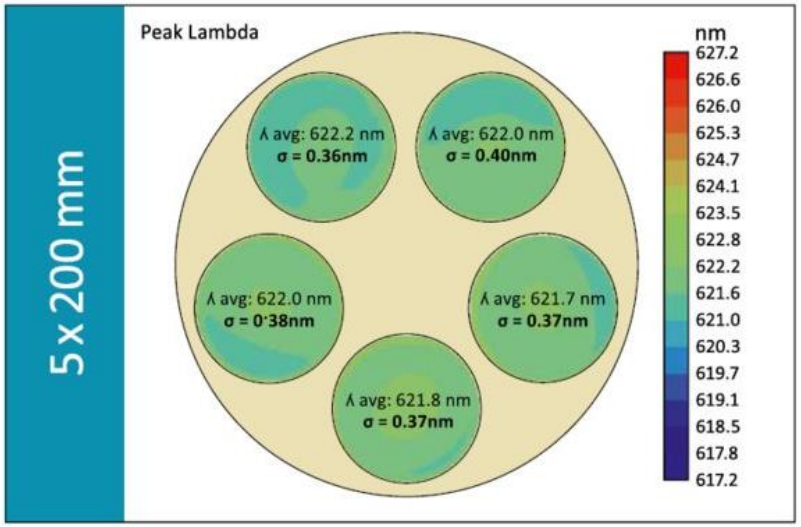
04 Epi. / Chip Fabrication

Epi. Equipment

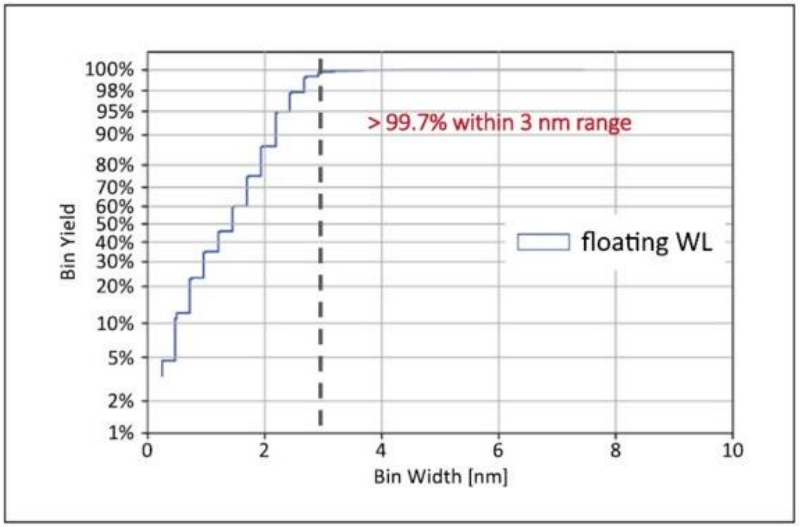
MOCVD : AXITRON G10-AsP

8 x 150 mm

5 x 200 mm



PL Plot – Fully Loaded microLED Run (5 wafers)



Bin Yield (%) for all wafer area (21 x 200 mm wafers)

* Source : AXITRON

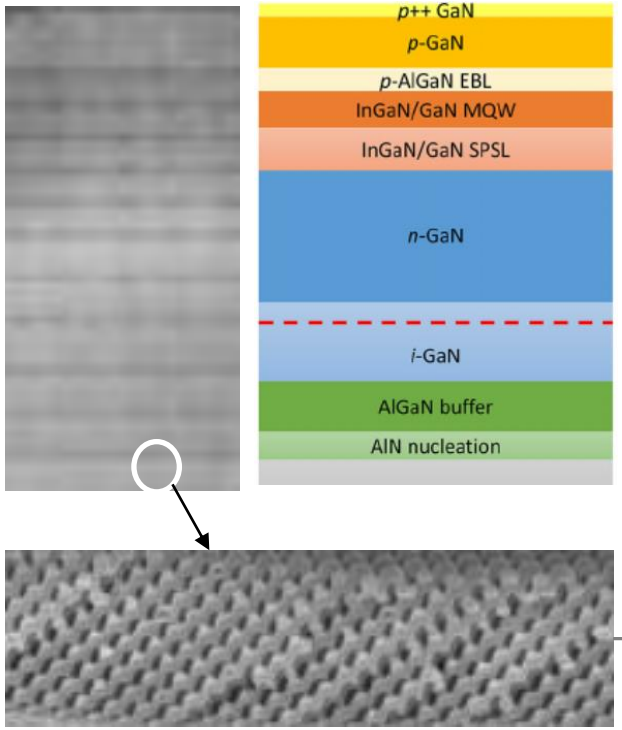
04 Epi. / Chip Fabrication

Epi. quality by epi. materials

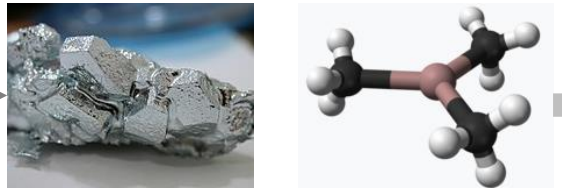
Gallium & Indium precursor in 6N purity level (99.9999%)

- The purity level and the process capability has been not verified for high qualified production of Micro LED and Nano LED

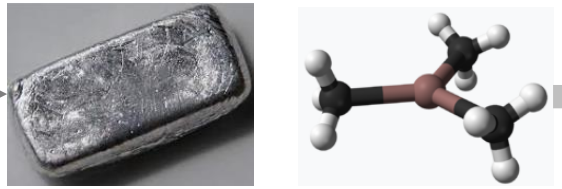
[Epi. Structure]



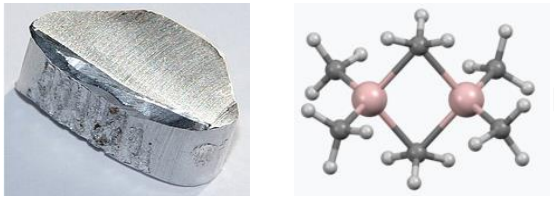
[Ga → TMGa(130 ~ 136 pm)]



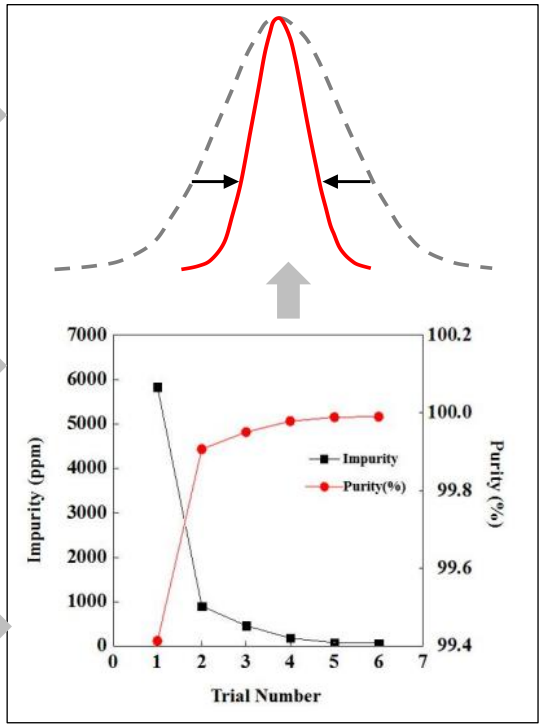
[In → TMIn(155 ~ 156 pm)]



[Al → TMA(118 ~ 125 pm)]



[Quality & Capablity]



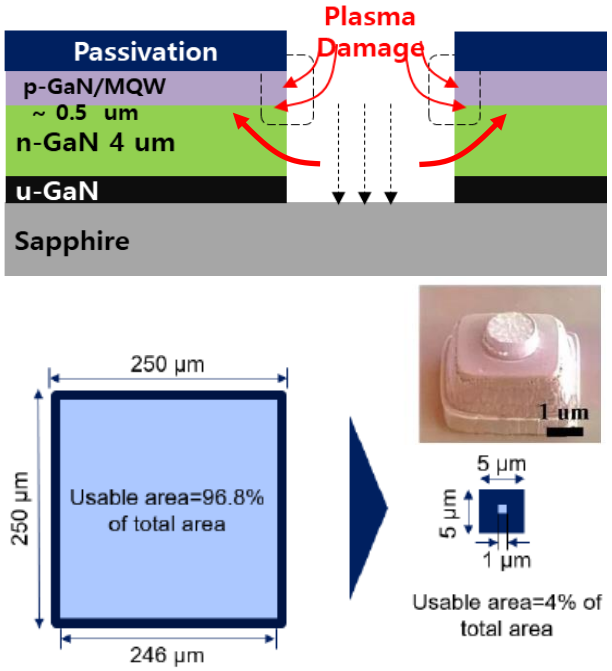
* Source : Yole Development, IDTech EX Research

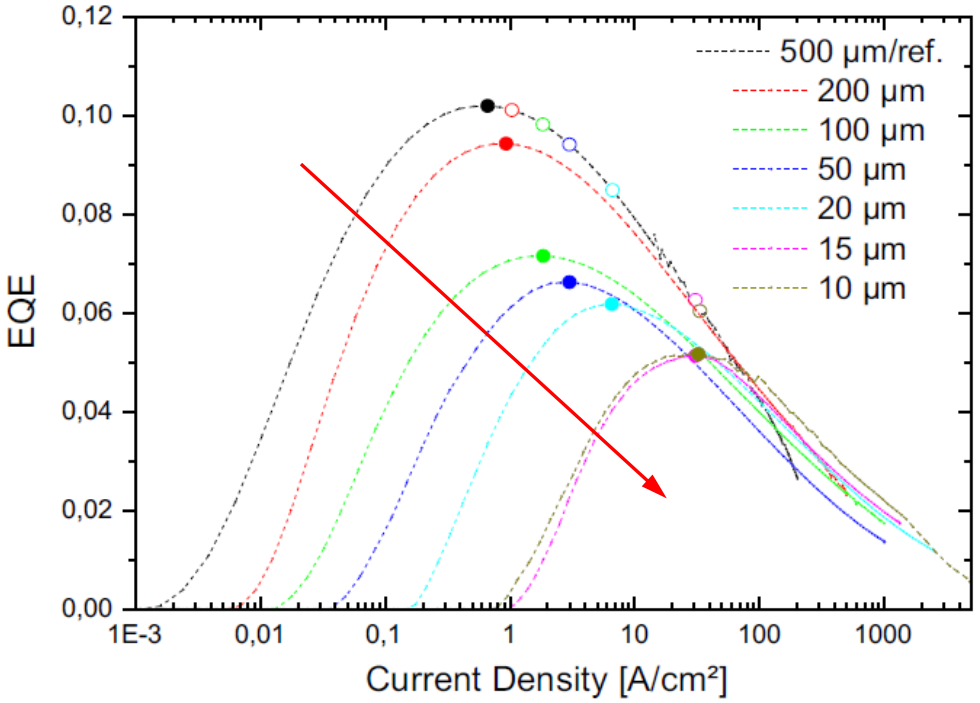
04 Epi. / Chip Fabrication

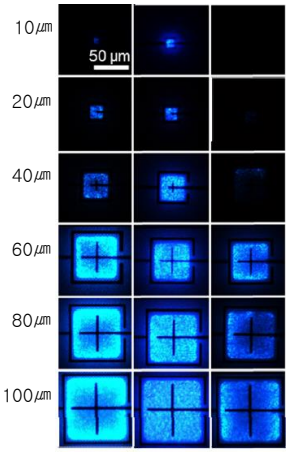
Efficiency Droop

Side Wall Effect → Non-Radiative Recombination Emission

- Open bonds, chemical contaminations, and structural damages from the dry-/Wet-etching process
- Sidewall effects can spread over distances similar to the carrier diffusion length, typically 1-10μm. μLEDs which have similar dimensions are therefore very sensitive





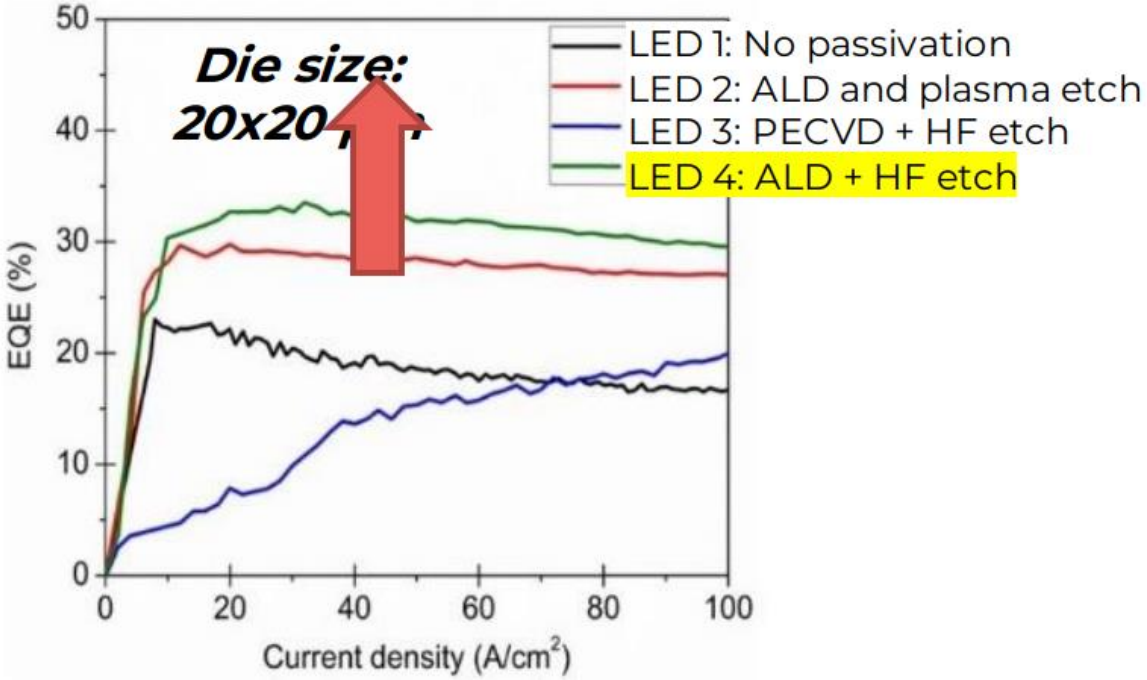


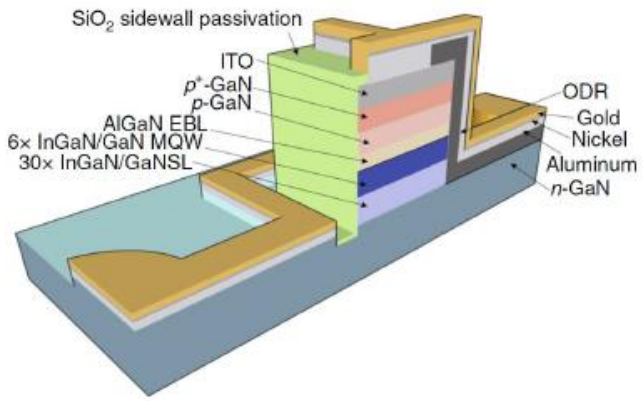
* Source : Yole Development, IDTech EX Research

04 Epi. / Chip Fabrication

ALD Passivation

- **Atomic layer deposition (ALD) technique to deposit a SiO_2 layer for sidewall passivation, together with KOH chemical treatment followed after.**
  - The electroluminescence images of the μLEDs (sizes from 10 μm to 100 μm) before and after sidewall passivation, as well as the EQE distribution clearly show the effect of treatment, which significantly improved the device performance.

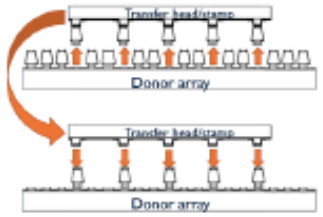
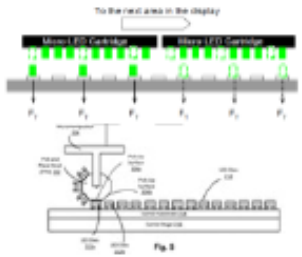
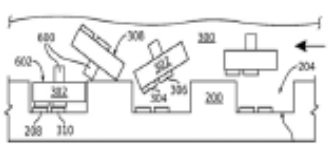




* Source : Yole Development, IDTech EX Research

05 Transfer & Bonding

Transfer Technologies

Process Type	Stamp / medium	Die pick up & holding	Die release & positioning forces
Deterministic			*From donor wafer & from transfer head*
Massively Parallel Pick And Place  A transfer head or 'stamp' goes back and forth between a donor and receiver wafer and carries thousands of chips that are transferred simultaneously with high accuracy.	**Silicon MEMS** *LuxVue-Apple, Mikro Mesa, PlayNitride, LG Electronics, AU Optronics, Innolux, San'an …*	Electrostatic	Electrostatic
	Elastomer *U of Illinois, X-Celeprint, Semprius, Cooledge, AUO, CSOT, ITRI, Oculus, Sanan…*	Magnetic / Electromagnetic	Electromagnetic Laser
Sequential / Semi Continuous Placing  Large numbers of chips in a 'bank' or chip carrier are 'printed' sequentially individually or in small groups. Alternatively, the transfer proceeds directly from the donor substrate and dies are individually released by a laser lift off process.	**Adhesive Tape** *PlayNitride, Intel, Goertek. Mikro Mesa, AUO, Samsung, Ultra Display Tech, Uniqarta…*	Adhesive	Thermal Mechanical
	Direct from LED wafers *Glo, Goertek, Tesoro…*		
	Clamping, Nozzles, Others [1] *BOE, CSOT, Facebook, Verlase, Point Engineering, Toray…*	Van Der Waals	Van Der Waals
Non Deterministic			
Self Assembly  LED dies are suspended in a fluid or electromagnetic field and position themselves in a non-deterministic fashion on specific sites, guided only by gravity and/or electromagnetic forces.	**Fluid** *eLux, Innolux, PARC, Samsung/PSI, Glo, Corning, Microsolar …*		Gravity Shape capture Vibrations Electrostatic/ magnetic
	Air / Gas *Self Array, Goertek*		

* Source : Yole Development, IDTech EX Research

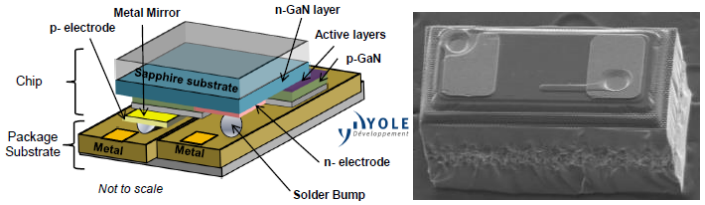
05 Transfer & Bonding

Transfer Technologies

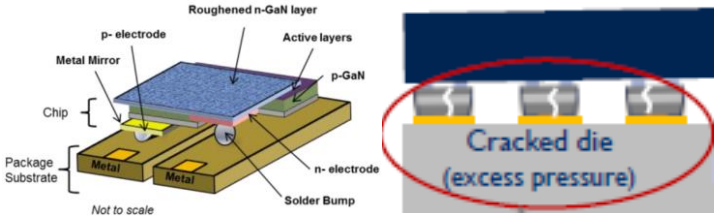
Chip structure for assembly

- Flip-chip → Vertical chip : Pick & Place → Self Assembly because of smaller size, bonding process

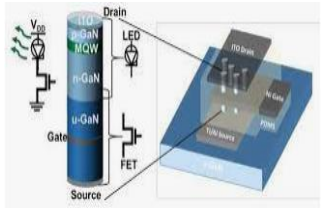
[Flip-Chip with template]



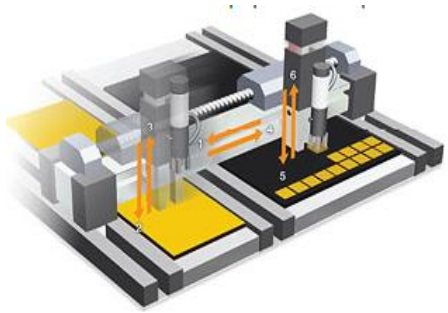
[Flip-Chip without template]



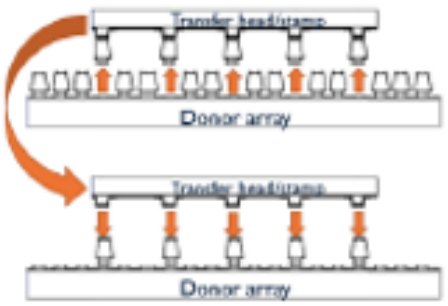
[Vertical Type]



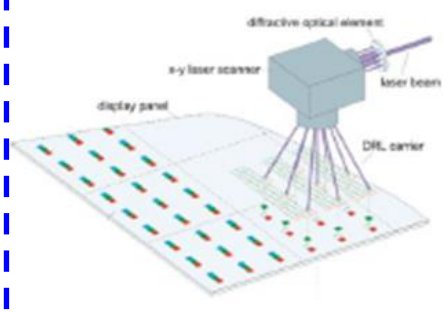
[Pick & Place]



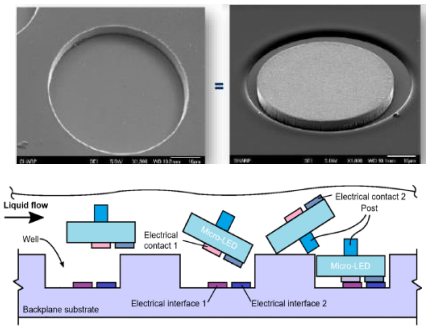
[Massively Pick & Place]



[Laser Assembly]



[Self Assembly]



* Source : Yole Development, IDTech EX Research

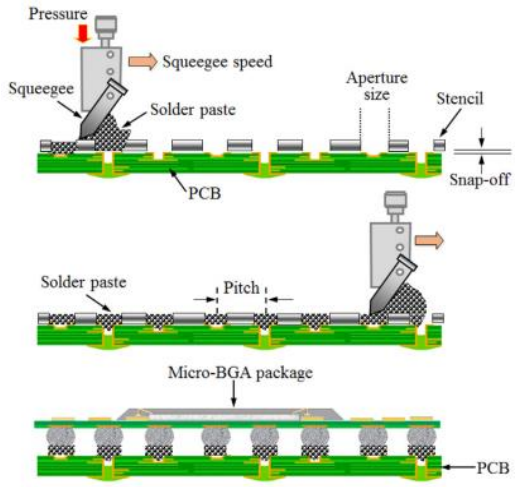
05 Transfer & Bonding

Bonding Technologies

Flip-Chip
Size : > 100 um

Panel Level

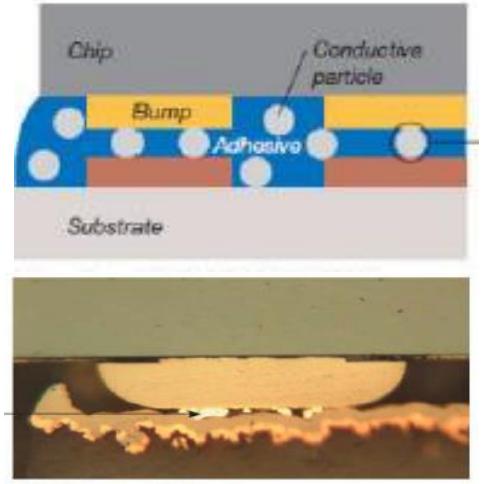
Solder Printing



Flip-Chip/Vertical
Size : < 50 um

Wafer Level

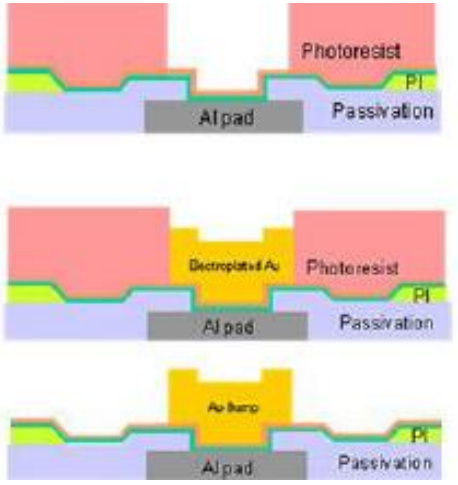
Adhesive Bonding



Flip-Chip : < 15 um
Vertical : < 5 um

Wafer+Panel Level

Electroplated Bump



Thermal-Compressive / Laser Assist Bonding

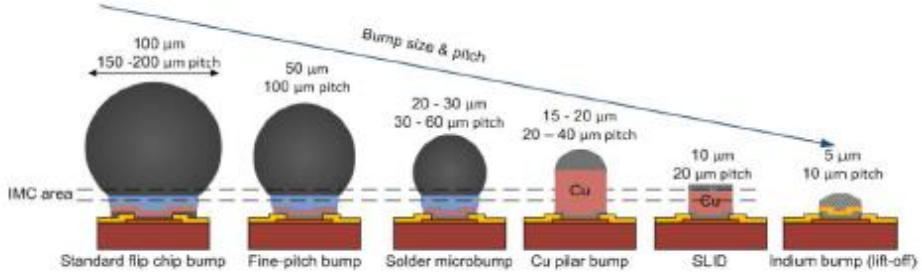
* Source : Yole Development

05 Transfer & Bonding

Bonding Technologies

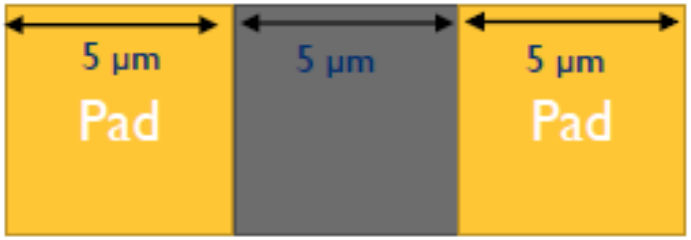
Bonding Solution : Micro bump Interconnect based on solder deposition

- The limiting factor in term of die size is therefore the interconnections : The minimum pad area is 5x5µm and the space between pads ~5 µm as well (i.e. : the pitch is 10µm)
- Can be the master solution of all Micro-LED display manufacturing ?

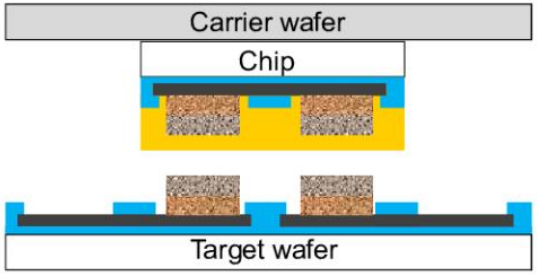


Evolution of traditional semiconductor packaging bumping requirements

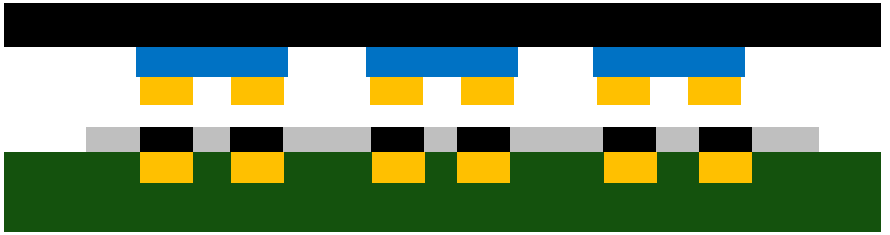
Source: Sami Vahanen–Advacam/CERN –ESE 2010



[Plated Bump + NCF + Laser]



[Pre-Aligned Conductive Adhesive]



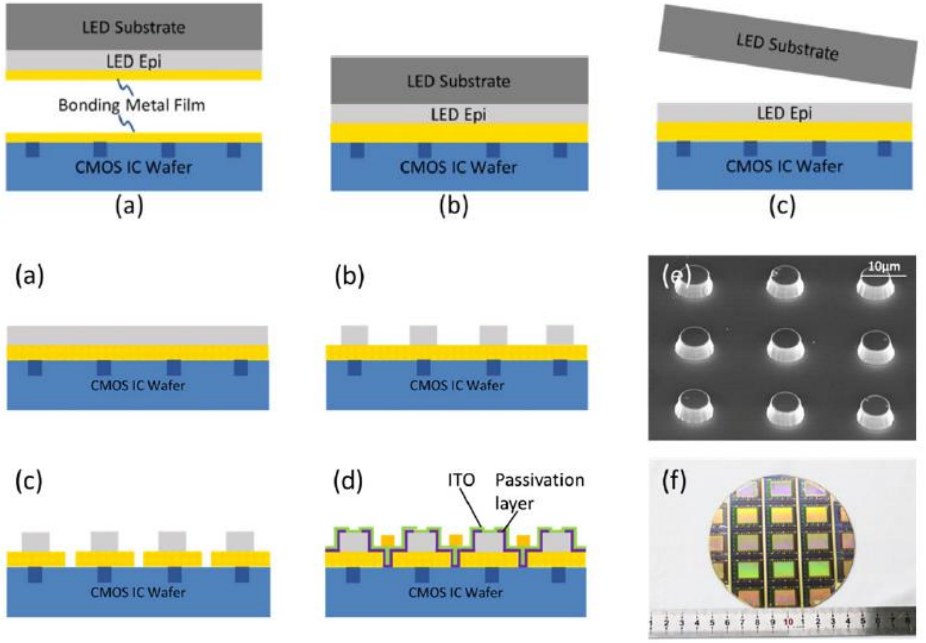
Source : Yole Development 2019

Tak F, et.al., "Non-conductive film and compression molding technology for self-assembly-based 3D integration",

06 Monolithic Integration

Panel Fabrication at Wafer Level

- RGB µLED on the wafer or selectively transfer substrate is bonded onto CMOS substrate
- Passivation and metal circuit is fabricated after the transfer & bonding process



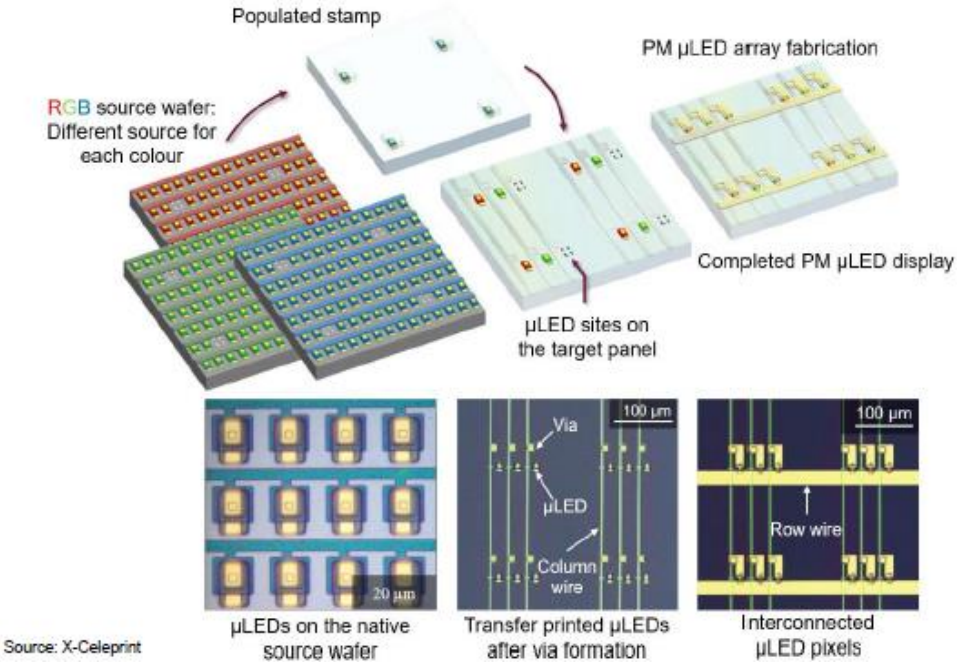
* Source : Yole Development, IDTech EX Research

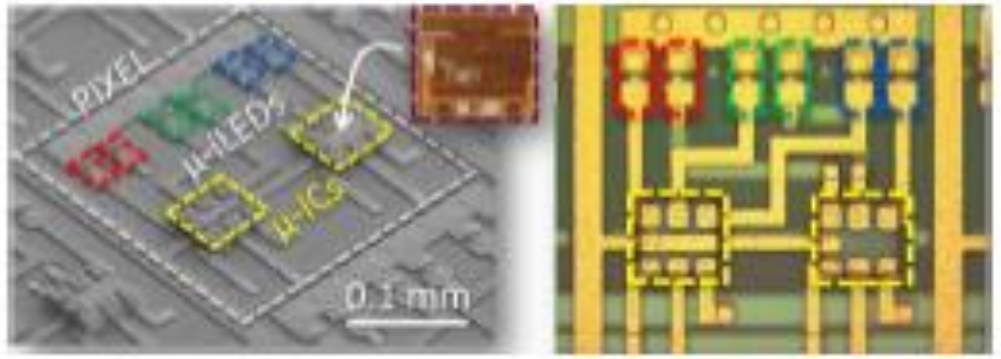
06 Monolithic Integration

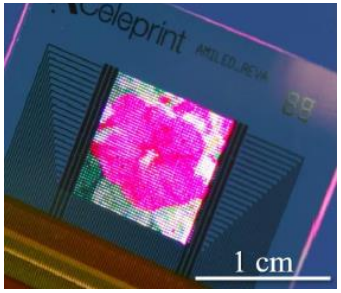
Panel Level : Monolithic Integration

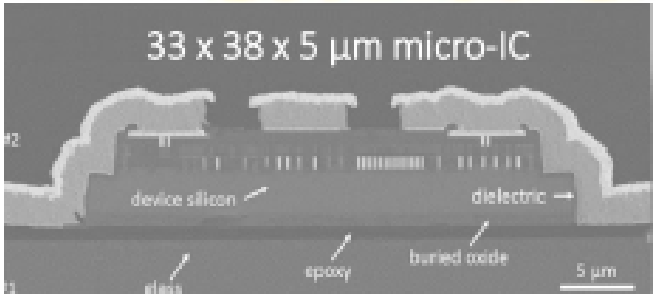
X-Celeprint & X-Display

- The display substrate is pre-patterned with column wires and µLEDs are transferred to the display substrate by elastomeric stamp. After transfer, standard photolithography and reactive ion etching (RIE) opens a via and finally the formation of a second metal level connects each µLED anode to each driver segment and also provides the row wiring to the cathodes of the µLEDs of the array.







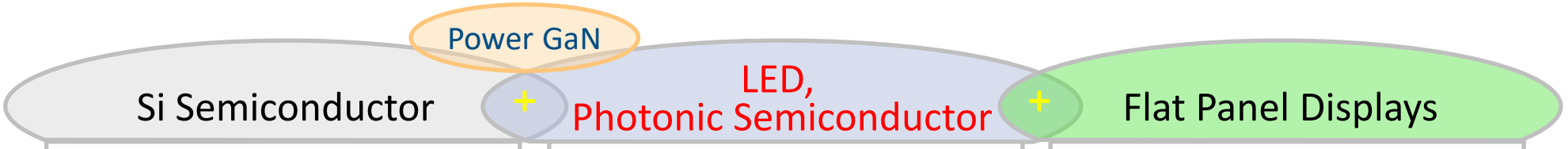


Source : IDTech 2020 Micro LED Displays

07 Conclusion

Disruptive Technologies and Processes

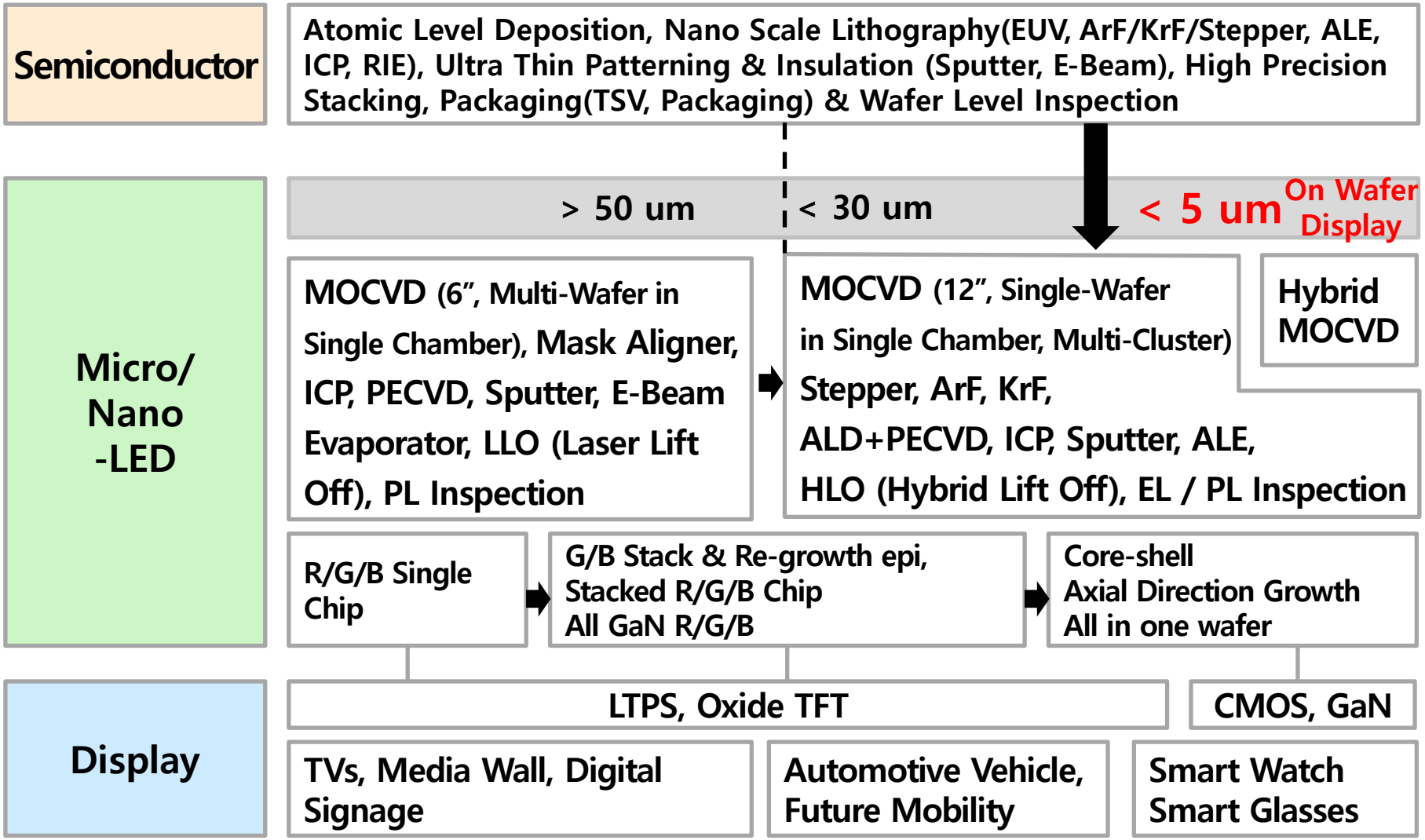
- **MicroLED display manufacturing can leverage many existing equipment and technologies from the display, semiconductor, and LED industries.**



Si Semiconductor	LED, Photonic Semiconductor	Flat Panel Displays
- CMOS foundries : backplanes or microdrivers. - Packaging processes : TSV, TGV, Bonding. - EOL Inspection and metrology Tools. - Munufacturing System : high-volume wafer processing, outstanding quality control, and yield management expertise	- Fairly mature MOCVD epitaxy tools → Need New System - Chip Process → Higher Precision Lithography Equipment - Wafer inspection, Electric & photoluminescence, etc - High placement accuracy chip bonding (VCSELs, photonics components assembly), more bonding techniques.	- TFT arrays + inspection, testing, repair. - Panel testing (chroma, mura…). Panel repair. - Driving, compensation. Modules, SOCs. - QD patterning and deposition (likely QD-OLED)

02 Conclusion

Disruptive Technologies and Processes



07 Conclusion

Market

Driving Forces

- New Market : Boundless Display Service → Beyond TVs
- Creation Market : AR & MR → Very Long time, High Brightness Solution
- Unique Market : Window Display, Automotive Display, Outdoor Display

Huddles

- Unstable Supply Chain, Mega Investment Vs. Small Cash-Cow
- Needs the cooperation between LED, Semi. & Display Industry

Technology

New Technologies

- Almost perfect pixel and panel fabrication processes for display such as epitaxial, deposition, dry etch, transfer, inspection etc.

Different Fabrication Method by Application (Chip Quality → Over 7N)

- Large Display for TVs, Video Wall → Modular and one panel type based on assembly process
- Small and Micro Display for smart watch and smart glasses → Wafer level process

감사합니다.

Not Post-OLED !!
New Market Creator